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Investigation of Modular Multilevel Converter Performance under Non-Ideal Distribution System Conditions

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INVESTIGATION OF MODULAR MULTILEVEL CONVERTER PERFORMANCE UNDER NON-IDEAL DISTRIBUTION SYSTEM CONDITIONS

by

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DEDICATION

This dissertation is dedicated to my Family.

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ABSTRACT

The Modular Multilevel Converter (MMC) is an emerging power converter technology that has caught widespread attention mainly because of several technical and economic benefits such as modular realization, easy scalability, low total harmonic distortion, fail-safe operations etc. The MMC is comprised of a series connection of sub-modules (SM). A sub-module is made by either a half-bridge or a full-bridge IGBT device and a capacitor as a source of energy connected across the bridge. This modular structure allows for the possibility to design high-voltage converters handling hundreds of kilo-volts without direct series connection of the power semiconductor devices.

Due to its modular and safe-fail structure, ability to work at low switching frequency (few hundreds of Hz) and reduced filtering requirements the MMCs are suitable for utility applications. One of the main challenges of a utility MMC is operation under non-ideal grid supply conditions. This includes phase to phase faults, phase to ground faults, non-sinusoidal grid supply etc.

This dissertation presents a novel control strategy for MMC based on frequency domain decomposition of the converter currents. The converter supply voltage is also decomposed into symmetrical components. By using the positive sequence grid voltage component as a reference voltage the control system can produce symmetric sinusoidal phase currents under any type of grid unbalance condition. A novel circulating current

controller based on frequency domain decomposition of arm currents is also presented which minimizes DC bus current ripples during unbalance grid supply

A novel and simple method for estimating operating region of certain MMC parameters as a function of input variables (grid voltages and power references) is developed. The function of the operating region with respect to key system parameters ensures that the operating region can be maximized

Finally, a new simplified loss modeling technique and a power reference computation algorithm is developed in order to extend its operating limit under certain unbalance conditions. The presented control architecture with a simplified real-time loss modeling method assures the best possible performance of a MMC during non-ideal supply conditions.

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LIST OF ABBREVIATIONS

AC……...Alternating Current

ADC……..Analog to Digital Converter

CPC……Current's Physical Components

DSP……Digital Signal Processor

DC…..……Direct Current

emf…...……Electro-Motive Force

IGBT…….……Insulated Gate Bipolar Transistor

MMC……Modular Multi-level Converter

N_{ON}…….....Number of sub-modules to be turned on

PI……...Proportional Integral

PR……...Proportional Resonant

PSC-PWM……...Phase-shifted Carrier-based PWM

PWM……...……Pulse Width Modulation

RDFT…….…...Recursive Discrete Fourier Transform

RMS……Root Mean Square

VB……..……..Voltage Balancing

VSC…….……Voltage Source Converter

THD……Total Harmonic Distortion

CHAPTER 1

INTRODUCTION

The Modular Multilevel Converter (MMC) concept was introduced over a decade ago by Lesnicar and Marquardt[1]. It is a promising technology that has caught the attention of many research groups in industry and academia, because of several technical and economic benefits such as modularity, scalability, low voltage distortion, failsafe operations etc.

Modular Multilevel Converters consist of series connections of sub-modules (also called static cells). This modular structure permits design of high-voltage converters handling hundreds of kilovolts without direct series connection of the power semiconductor devices as in two or three level converters. Additionally, the large number of voltage levels reduces the filtering requirement on both DC and AC side of a converter even at very low switching frequency.

Figure 1.1 shows the classification of three-phase MMCs based on sub-module (SM) structure (half bridge or full bridge) [2]. In general MMCs can be classified into:

1) Star configured MMC
2) Delta configured MMC
3) Double star-configuration MMC

a) Half-bridge MMC

b) Full-bridge MMC

4) The dual MMC

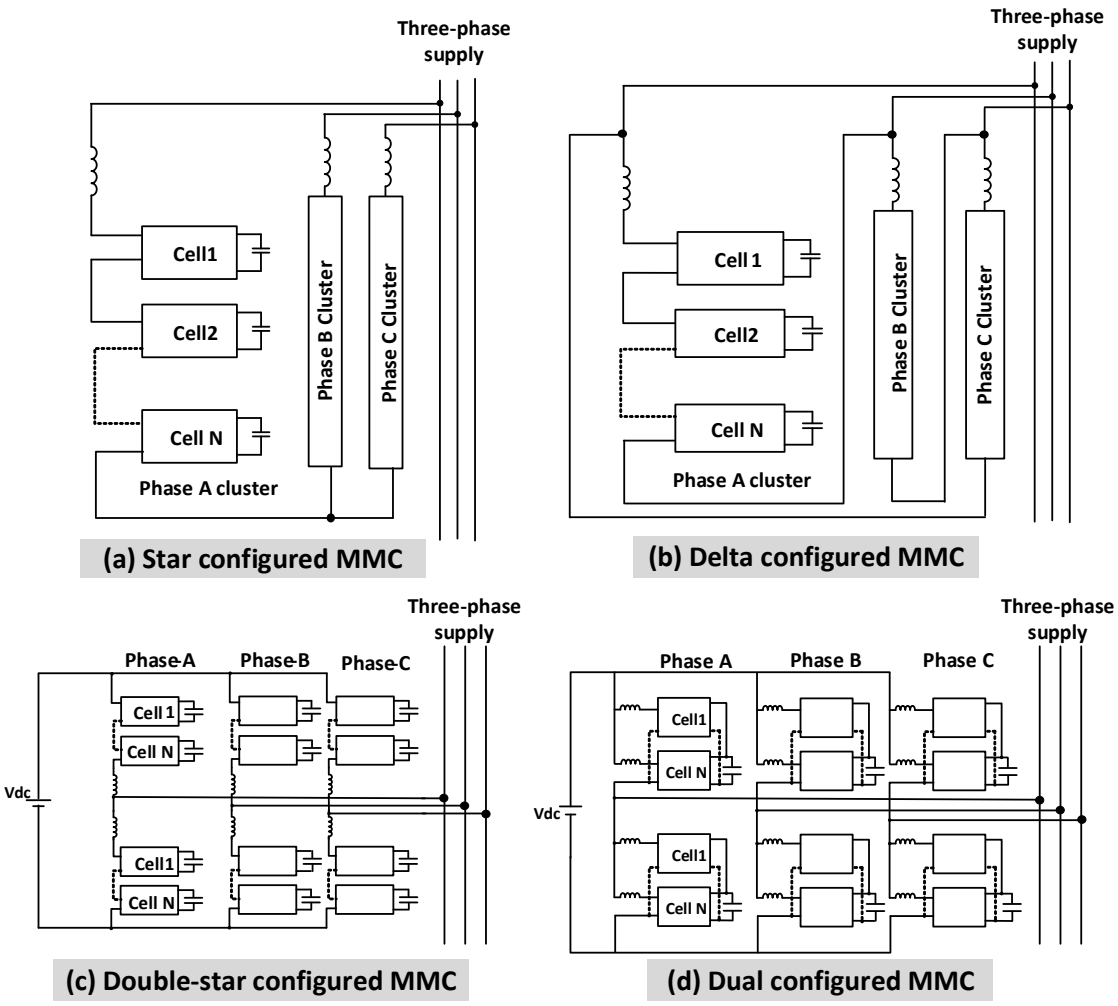

Figure 1.1 Circuit configurations of MMC (a) Star configured MMC (b) Delta configured MMC(c) Double star Configured MMC (d) The Dual MMC

Figure 1.1 (a) & (b) shows the star/delta-configured MMC topology. These configurations do not have common dc-link terminals and therefore these star-delta configurations mostly find applications in STATCOMs and energy storage systems [3]. Figure 1.1 (c) shows the double-star-configured MMC topology which possesses a common dc-link. Due to its structure this configuration can be used for interfacing AC

and DC system for achieving bidirectional power transfer between those systems. Therefore the double-star topology is highly suitable for utility related converter applications. Another MMC topology is shown in Figure 1.1 (d) which is called Dual MMC. In this case, each dc side of positive and negative chopper-cells possesses a common dc capacitor, whereas its ac side is connected in parallel via buffer inductors. It is mainly used for low-voltage large-power conversion applications [3].

The double-star MMC configuration, which is the most suitable for utility applications, needs to handle various grid supply related issues such as phase-to-ground faults, phase-to-phase faults, non-sinusoidal supply caused by harmonic generating loads, etc. A control strategy must be provided that protects MMC systems and delivers the best possible performance during such non-ideal AC grid conditions. In order to achieve that, a novel method for control of double-star topology MMCs under non-ideal AC side conditions is presented in this dissertation. The dissertation outlines a traditional control method in chapter 2 and elucidates the limits of such control systems under non-ideal supply conditions in chapter 3. A new control strategy is presented in chapter 4 that achieves the desired performance criteria during unbalance supply conditions and then chapter 5 develops a novel method for estimating and extending the operating region of a MMC during asymmetrical supply conditions. The traditional control method described in chapter 2 serves as the baseline of comparison for validating the performance of the proposed control method.

CHAPTER 2

MODELING AND TRADITIONAL CONTROL OF MODULAR MULTILEVEL CONVERTERS

This chapter describes dynamic modeling of the double star MMC configuration and selection of its passive elements. It also provides a background literature survey on MMC control methods and then develops a commonly used control approach along with simulation results.

2.1 OVERVIEW OF DOUBLE-STAR CONFIGURATION MMC

Figure 2.1 shows a three-phase MMC double-star structure using half-bridge IGBT sub-modules. A six-level half-bridge MMC will be investigated in this dissertation for achieving various performance objectives. Although more many more levels are typically used, six levels are sufficient for investigations without loss of generality and match a hardware laboratory prototype that is available for future validation of this work. The following section focuses on developing a mathematical model of a double-star MMC and design of the commonly used closed loop control system for MMCs used in utility applications.

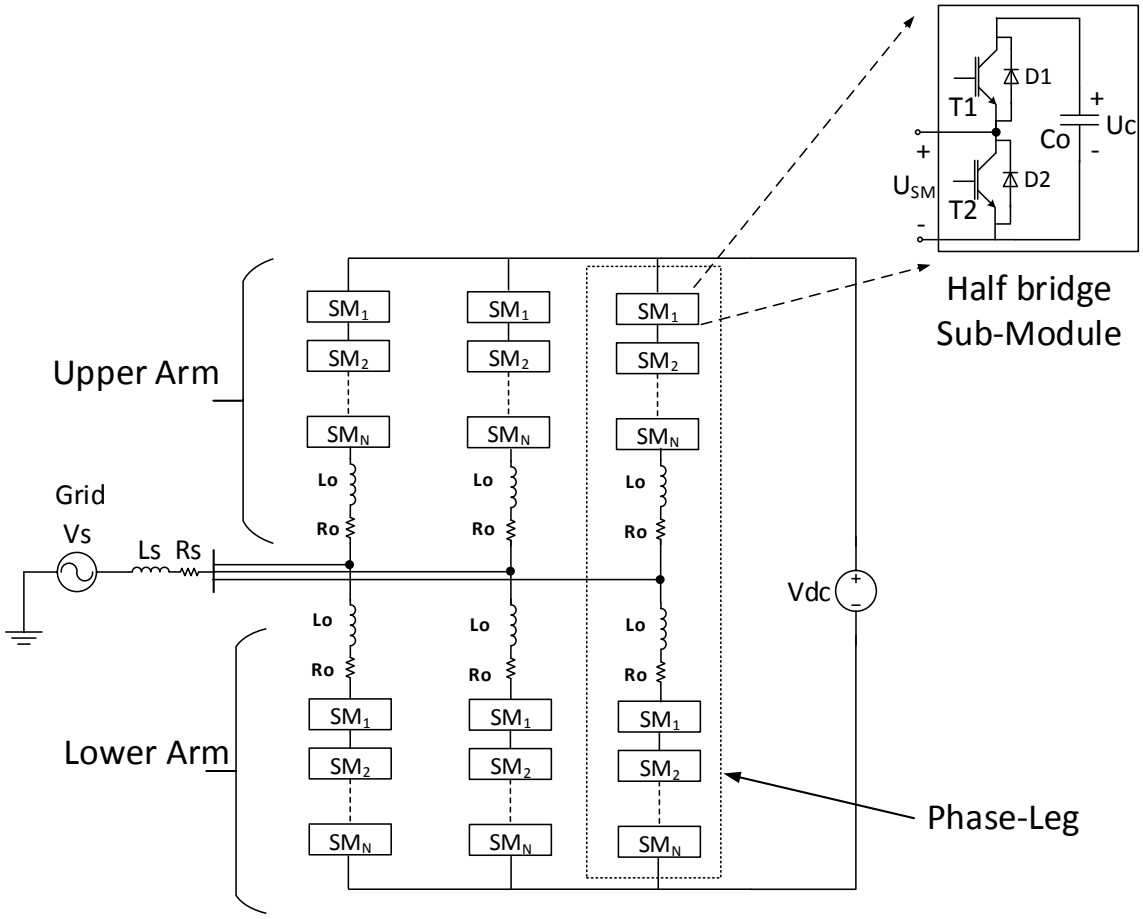

Figure 2.1 Half-bridge three-phase Modular Multilevel Converter

2.2 MMC MODELING

Various modeling methods have been explored in the literature for targeted applications of the MMC. For modeling purpose many authors assume that voltage across each sub-module capacitor remains ideal. This assumption helps to derive simple dynamic equations of the MMC. Without this assumption modeling would be much more complicated because of the different voltages across each sub-module caused by bidirectional current flowing through them.

Reference [4] derives a continuous domain model of a MMC by representing the system with ordinary differential equations which are then solved by numerical integration methods. The continuous model accurately describes lower order harmonics. Frequency domain approaches have been attempted by [5] & [6]. Reference [5] decouples the MMC circuit into separate AC and DC parts using linear transformation and then the sub-module variables are computed using iterated convolution. The method is used with an optimization algorithm to extend the operating region of MMC for given grid and converter parameters. The analysis and prediction of harmonic content in arm currents and sub-module capacitors was investigated in the frequency domain by the application of Fourier series in [6].

Other modeling approaches have been proposed in references [7], [8], [9], [10], [11], [12]. In general, there are three main parameters to be considered for MMC modeling: arm currents, output currents and sub-module capacitor voltages. Reference [11] has proposed a modeling method based on energy stored in the upper and lower arms of each phase. The mathematical equations for total energy in an arm and difference between upper and lower arm energy are derived and used for control purpose. Whereas, a switching function based modeling technique is implemented by [12].

In this dissertation the MMC dynamics are derived based on [10] & [11] since it covers various aspects of MMC design and simulation. The model mainly focuses on arm current, sub-module capacitor voltage and circulating current dynamics. These dynamics are formulated by using first order differential equations of arm currents and inner difference voltages of each phase. In order to develop the model consider Figure 2.2 which shows the detailed circuit of the three-phase MMC where Lo and Ro are the arm

inductance and equivalent resistance respectively. *Vdc* and *Idc* are total DC side voltage and current respectively. The MMC output voltage is denoted by U_{vj} and phase currents are denoted by i_{vj} where $j = a,b,c$. The arm voltage generated by cascade connection of Sub-modules is expressed by U_{pj} and U_{nj} where the sub-script $p \,\&\, n$ refers to the upper and lower arm respectively.

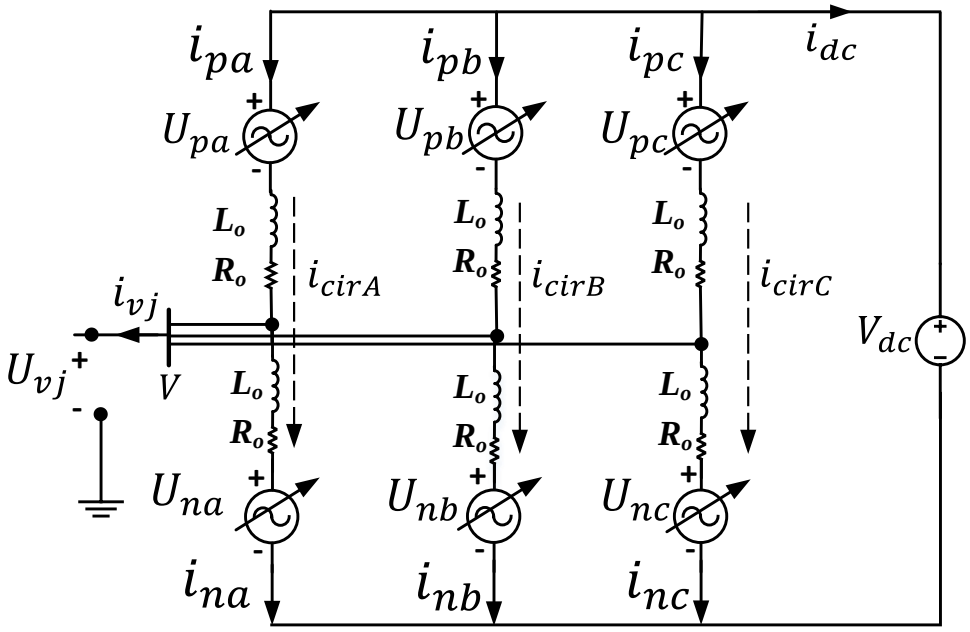

Figure 2.2 MMC with equivalent circuit of sub-modules

From Figure 2.2 the upper and lower arm currents $i_{pj} \,\&\, i_{nj}$ can be expressed as

$$i_{pj} = i_{diffj} + \frac{i_{vj}}{2} \tag{2.1}$$

$$i_{nj} = i_{diffj} - \frac{i_{vj}}{2} \tag{2.2}$$

Where i_{diffj} represents the difference current or circulating current of phase j which flows through both upper and lower arms and it is expressed as average of both upper and lower arm currents,

$$i_{diffj} = \frac{i_{pj} + i_{nj}}{2} \tag{2.3}$$

According to [10] & [11] the MMC can be characterized by equations (2.4)-(2.9).

Output voltage is given by,

$$Uvj = e_j - \frac{Ro}{2}.i_{vj} - \frac{Lo}{2}.\frac{di_{vj}}{dt} \tag{2.4}$$

DC loop equation of each MMC arm is given by,

$$Lo.\frac{di_{diffj}}{dt} + Ro.i_{diffj} = \frac{U_{dc}}{2} - \frac{u_{pj} + u_{nj}}{2} \tag{2.5}$$

Inner emf generated in phase 'j' is given by,

$$e_j = \frac{u_{nj} - u_{pj}}{2} \tag{2.6}$$

According to equation (2.4) the output phase current i_{vj} can be directly controlled by regulating control variable e_j. This allows to use a current vector control scheme based on $d-q$ coordinates which ideally guarantees zero steady-state error.

Inner difference voltage of phase j is given by,

$$u_{diffj} = Lo.\frac{di_{diffj}}{dt} + Ro.i_{diffj}$$

$$u_{diffj} = \frac{U_{dc}}{2} - \frac{u_{pj} + u_{nj}}{2} \tag{2.7}$$

Equation (2.7) shows that the difference current i_{diffj} can be controlled by regulating difference (unbalance) voltage u_{diffj}.Therefore from equations (2.6) and (2.7) the reference voltages for upper and lower arms are derived as give below:

$$u_{pj\_ref} = \frac{U_{dc}}{2} - e_j - u_{diffj} \tag{2.8}$$

$$u_{nj\_ref} = \frac{U_{dc}}{2} + e_j - u_{diffj} \tag{2.9}$$

The circulating current is generated by the voltage imbalances among each phase leg and it is mainly composed of negative sequence 2nd harmonic component [10]. In equations (2.8) and (2.9) it the same difference voltage (which is mainly responsible for circulating current) is subtracted from both the upper and lower arm voltage references. Thus the resulting e_j will not change and the AC side dynamics are unaffected by the circulating current. However, the circulating current increases the RMS value of arm currents and therefore causes higher converter losses (through arm inductors, capacitors and semiconductors).

Ideally, in steady state, the circulating current should be zero, but because of leg voltage imbalances the circulating current would have a 2nd order harmonic current superimposed on the existing arm current. In the time domain, the circulating currents of three phases could be expressed as combination of DC and AC parts as given below,

$$i_{diffa} = \frac{I_{dc}}{3} + I_{2f}\sin(2w_o t + \varphi_o) \tag{2.10}$$

$$i_{diffb} = \frac{I_{dc}}{3} + I_{2f}\sin(2w_o t + \frac{2\pi}{3} + \varphi_o] \quad (2.11)$$

$$i_{diffc} = \frac{I_{dc}}{3} + I_{2f}\sin(2w_o t - \frac{2\pi}{3} + \varphi_o] \quad (2.12)$$

Where, I_{dc} is total DC current as shown in Figure 2.2. I_{2f} is the peak value of 2nd harmonic circulating current, w_0 is the fundamental frequency and φ_0 is the initial phase angle.

According to [13] and [14] three-phase currents can be transformed into two dc components by applying the Park transformation to the three phase current equations. This transformation is also known as a-b-c to d-q transformation. The transformation is done on fundamental line frequency rotational reference frame for phase currents whereas on double line frequency negative sequence rotational reference frame for circulating currents. The Park transformation matrix is given by,

$$T_{acb/dq} = \frac{2}{3}\begin{bmatrix} cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \quad \dots (\theta = 2w_{ot}\mathrm{t}) \quad (2.13)$$

and corresponding inverse Park transformation is given by,

$$T_{dq/acb} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - \frac{2\pi}{3} & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \quad \dots (\theta = 2w_{ot}\mathrm{t}) \quad (2.14)$$

Equation (2.7) can be written in vector form as,

$$\begin{bmatrix} u_{diffa} \\ u_{diffc} \\ u_{diffb} \end{bmatrix} = Lo.\frac{d}{dt}\begin{bmatrix} i_{diffa} \\ i_{diffc} \\ i_{diffb} \end{bmatrix} + Ro\begin{bmatrix} i_{diffa} \\ i_{diffc} \\ i_{diffb} \end{bmatrix} \tag{2.15}$$

Substituting (2.10), (2.11) and (2.12) in (2.15) and applying the park transformation matrix of (2.13),

$$\begin{bmatrix} u_{diffd} \\ u_{diffq} \end{bmatrix} = Lo.\frac{d}{dt}\begin{bmatrix} i_{2fd} \\ i_{2fq} \end{bmatrix} + \begin{bmatrix} 0 & -2w_oL_o \\ 2w_oL_o & 0 \end{bmatrix}.\begin{bmatrix} i_{2fd} \\ i_{2fq} \end{bmatrix} + Ro\begin{bmatrix} i_{2fd} \\ i_{2fq} \end{bmatrix} \tag{2.16}$$

Here, u_{diffd} and u_{diffq} are $d-q$ components of difference voltage and i_{2fd} and i_{2fq} are $d-q$ components of circulating current. The $2w_0L_0$ and $-2w_0L_0$ terms show the cross-coupling between d and q axis components. By using (2.16) the transfer function block diagram of circulating current [10] can be represented as shown in Figure 2.3.

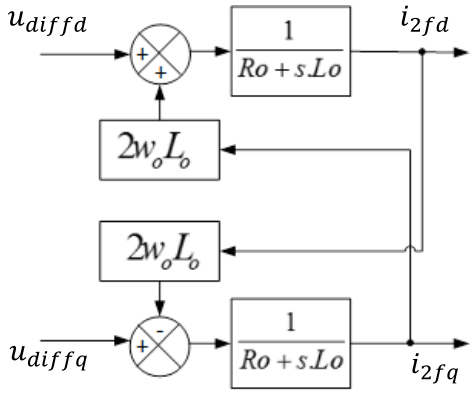

Figure 2.3 Circulating Current Transfer Function

2.3 SELECTION OF ARM INDUCTACE AND SUBMODULE CAPACITANCE

Two main aspects of MMC design are dimensioning of sub-module capacitors and arm inductors. In [15] a design principle is described for design of arm inductor

based on two distinctive functions: suppressing circulating current and limiting fault current rise rate. Reference [16] discusses dimensioning of SM capacitor for MMC by considering voltage limits of SM with voltage. Using [15] and [16] the selection of arm inductor and sub-module capacitor is done as shown below.

The formula for selection of sub-module capacitor is given by equation (2.17).

$$C = \frac{P}{3\,k\,N\,w_o\,e\,{V_c}^2}\left[1-\left(\frac{k\cos(\emptyset)}{2}\right)^2\right]^{\frac{3}{2}} \tag{2.17}$$

The formula for selection of arm inductance is given by equation (2.18).

$$L = \frac{1}{8\,{w_o}^2\,C\,V_c}\left[\frac{P}{3\,I_{2f}}+V_{dc}\right] \tag{2.18}$$

Given parameters are,

$$P = 60e3\text{VA};\ N = 6;\ w_o = 2\text{*pi*}60\frac{rad}{s};V_C = 133.33\text{V};\ Vdc = 800V;$$

$$I_{2f} = 15\text{A};\ k = 0.3;\cos(\phi) = 1;e = 10\%$$

For the above given parameters the sub-module capacitance is found to be 16.4mF. A choice was made to use 15mF based on market available capacitors size, cost, ESR and availability. Using 15mF as a sub-module capacitor now the arm inductance can be designed based on equation (2.18). The resulting value found for arm inductor is 0.938mH. A choice was made to use 1mH based on cost, size, weight and availability.

2.4 MMC CONTROL STRUCTURE

Figure 2-4 shows the block diagram of a typical control structure of a MMC. The control structure consists of three main components: multilevel modulation, voltage balancing algorithm and closed loop controllers for achieving desired power conversion objectives. The closed loop controller has three types of controllers namely, inner phase current controller, outer power controller and circulating current controller.

This section focuses on MMC modulation schemes, voltage balancing techniques and closed loop control approaches that have been implemented so far in the known literature. Based on the background research and literature survey a commonly used modulation, voltage balancing and controller design approach is selected to design a simulation model to understand the basics of MMC and issues related to control technique.

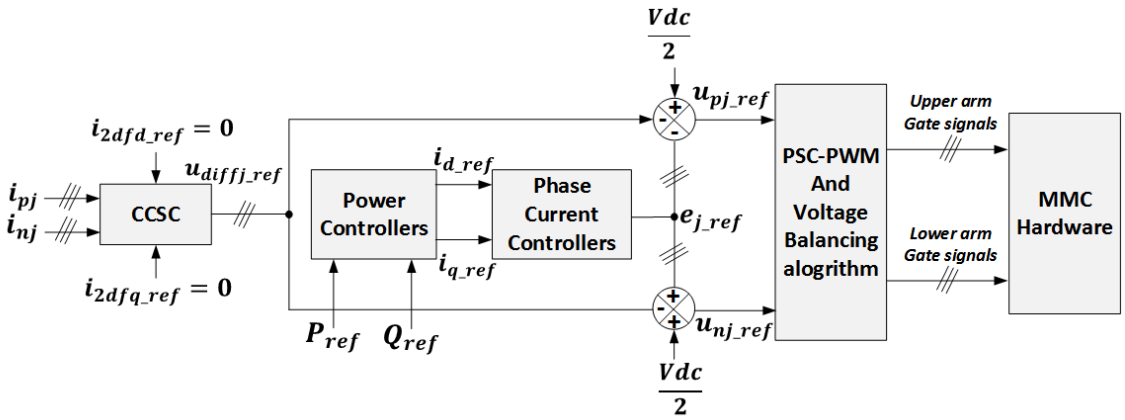

Figure 2.4 Complete control structure of a MMC

2.4.1 MULTI-LEVEL MODULATION TECHNIQUES

Various modulation techniques have been investigated over the last decade. Considering the MMC structure, the switching loss is directly proportional to number of

MMC levels; therefore switching frequency reduction technique has been the core of many modulation methods. Authors of [17], [18], [19] have implemented Sub-module Unified Pulse Width Modulation (SUPWM). Reference [17] implements SUPWM by using 180 deg. phase shifted carrier signal for upper and lower arms. This method achieves sub-module voltage balancing for single phase MMC without using a closed loop control for capacitor voltage balancing. However, the performance of this technique remains unknown for its extension to three-phase MMCs.

Another modulation scheme known as Carrier Shifted Pulse Width Modulation (CS-PWM) is implemented by references [20], [21], [22], [23], [24], [25]. The carrier shifted method is divided in two parts: Phase shifted and Level Shifted. In Carrier Phase Shifted PWM (CPSPWM) method 'N' carrier signals are used to create N+1 level inner emf. The phase shift between two consecutive carrier signals is equal to 360/N. Whereas in Level Shifted PWM (LSPWM) each carrier (out of N) has particular DC offset and addition of all carrier offsets is equal to peak amplitude of modulating signal. These two methods could also be combined to implement different variations of carrier shifted PWM such as Phase Disposition(PD), Phase Opposition Disposition(POD), Alternative phase opposition disposition (APOD), Saw-tooth etc. These methods use Sub-module capacitor voltages for close loop control of voltage balancing. Reference [23] implements another variation of carrier shifted PWM in which the modulating waveform is shifted and scaled to bring inside one carrier signal. With this technique the harmonics in the phase voltage are shifted to twice the switching frequency. Reference [1] has implemented a traditional space vector PWM (SVPWM) modulation technique. The

SVPWM method finds limited practical applications because the complexity of algorithm is proportional to the number of levels in MMC.

Apart from conventional modulation techniques some other ideas like fundamental switching frequency with predefined pulse pattern generation [26], stochastic optimal fundamental switching frequency [27] were also proposed.

This dissertation uses Phase Shifted Carrier PWM method for modulation purposes. A typical block diagram of PSC-PWM modulation scheme is shown in Figure 2.5.

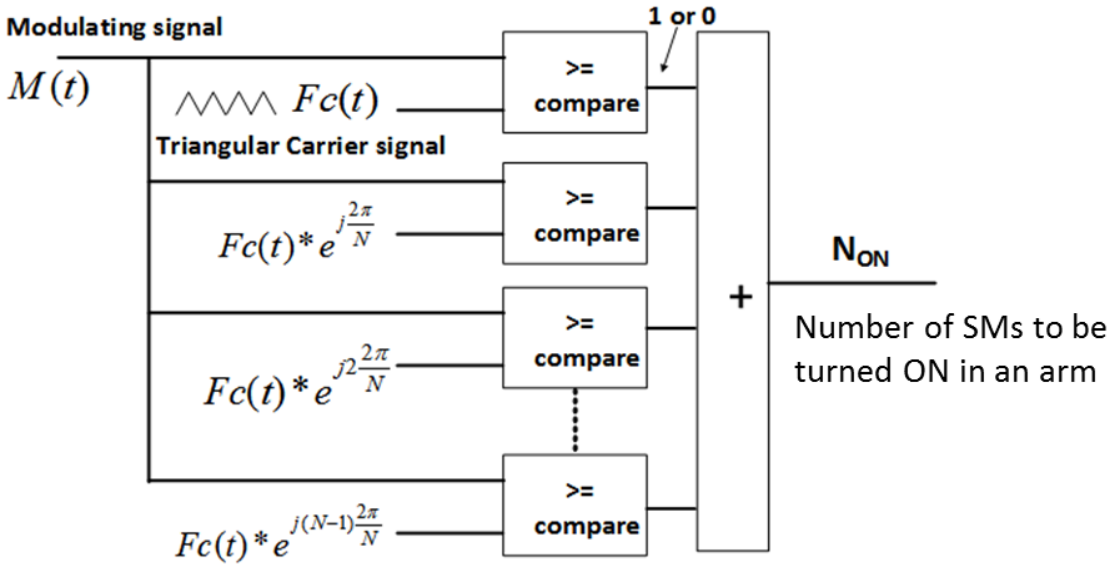

Figure 2.5 PSC-PWM modulation scheme block diagram

The structure is similar to a traditional sine-triangle modulation where a low frequency modulating signal (usually sinusoidal) is continuously compared with a high frequency triangular shaped signal (also called as a carrier signal). Due to nature of multiple levels in the converter more sine-triangle comparison blocks are required. The total number of compare blocks is equal to the number of sub-module in an arm of MMC. The

modulating signal is connected to all compare blocks as it is but the carrier signals are connected using different phase-shifts. For 'N' level MMC the phase shift between any two carriers is given by '360/N'. The result of the compare block is either 1 or 0. All the results are added together to produce a signal called as "N_{ON}" which means 'Number of sub-modules to be turned ON in that particular arm. Figure 2.6 shows an example of a six-level PSC-PWM with modulating signal and the resultant 'N_{ON}' signal.

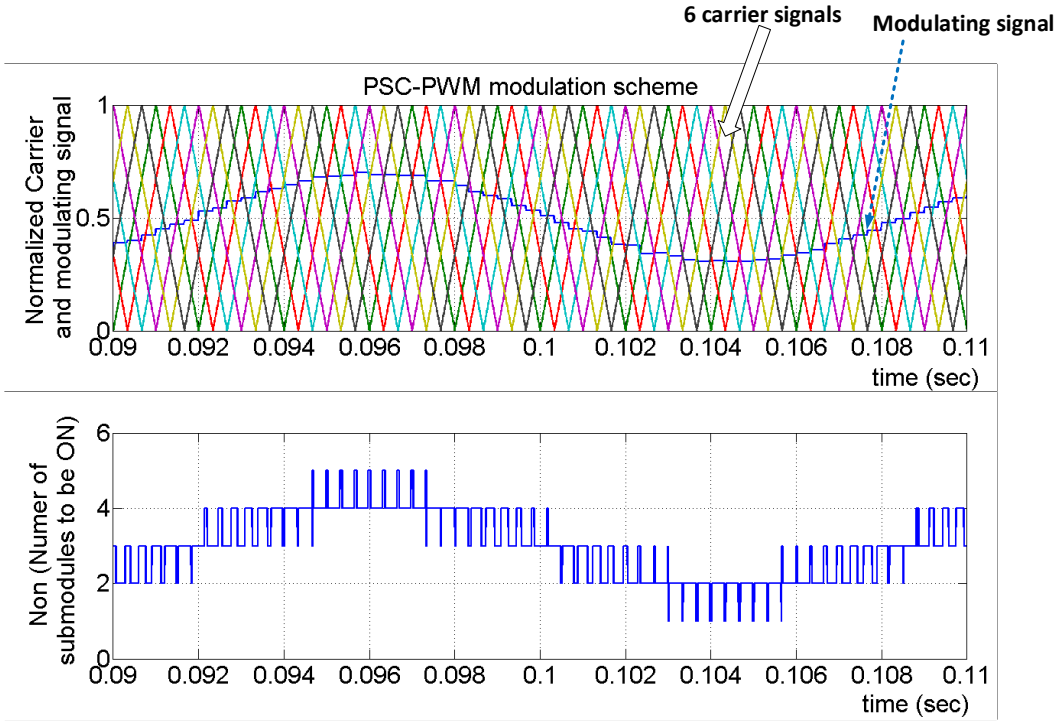

Figure 2.6 Six-level PSC-PWM with modulating signal

2.4.2 SUB-MODULE VOLTAGE BALANCING

Modular Multilevel Converter voltage imbalance between sub-module capacitors is a significant concern with MMCs. Based on the direction of arm currents the sub-module capacitors would charge or discharge causing the voltage across them to fluctuate about their nominal value. These fluctuations or ripples are proportional to the magnitude

of arm currents. The ripples are also affected by the modulation scheme, semiconductor switching frequency and system sampling frequency used. Many research papers have addressed voltage balancing issues in MMCs [28], [29], [30], [31], [32], [33] and [34].

There are in general two types of sub-module voltage balancing approaches in the literature: open loop and closed loop. In the open loop approach some voltage balancing compensation is added to the modulation scheme. This method does not use any feedback from sub-module capacitors. Whereas in the closed loop approach the sub-module capacitor voltages are measured and used as a feedback to make necessary adjustments in switching of sub-module semiconductors.

A new voltage balancing algorithm called as Reduced Switching Frequency (RSF) Voltage balancing was proposed by [10] for a 20-level MMC. In this technique the output of PSC-PWM modulation blocks (also known as N_{ON}, where N_{ON} means Number of Sub-modules to be turned on) is passed to the RSF-VB algorithm. The input parameters for RSF voltage balancing algorithm are upper and lower arm SM capacitor voltages, upper arm current, lower arm currents, upper arm 'N_{ON}' and lower arm 'N_{ON}'. Based on the direction of individual arm current the measured sub-module voltages are sorted in ascending or descending order. Then depending on the previous and current value of their 'N_{ON}' a decision is made whether to keep a sub-module as it is or to turn it ON or to turn it OFF. This technique allows reduction of the average switching frequency of a sub-module below the carrier frequency while keeping the sub-module capacitor voltages well balanced. But this type of reduced switching balancing is only effective if the MMC has a large number of sub-modules. For lower number of sub-modules,

reducing switching frequency further causes degradation of the performance of the voltage balancing algorithm.

In this dissertation a six-level MMC is investigated, therefore, to obtain good voltage balancing the conventional voltage balancing algorithm is used. The block diagram of modulation and voltage balancing scheme is shown in Figure 2.7 and the flow chart for the conventional voltage balancing algorithm is shown in Figure 2.8.

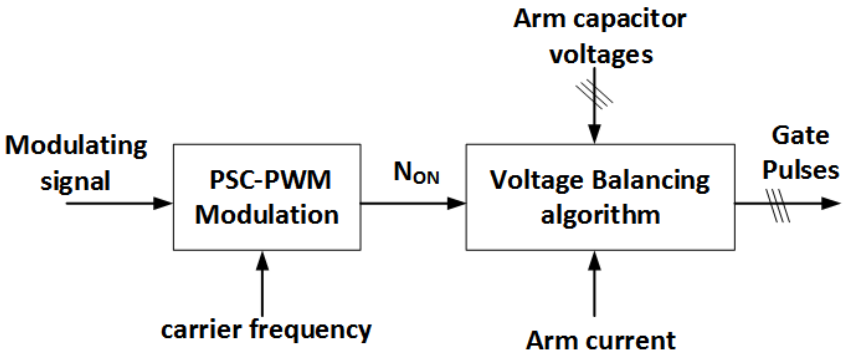

Figure 2.7 Block diagram of Modulation and Voltage balancing scheme

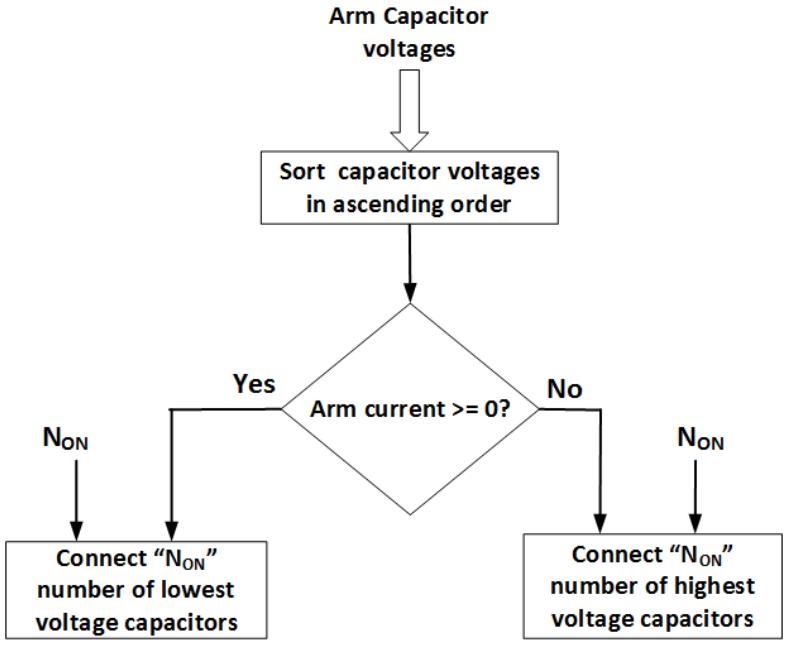

Figure 2.8 Conventional Voltage Balancing Algorithm

2.4.3 CLOSED LOOP CONTROLLERS DESIGN

Various MMC control methods have been investigated by references [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45]. Most authors assume balanced grid conditions when designing a control system for a MMC. In general there are three ways to approach the MMC control system design. The first approach is based on traditional inner current control and outer power/voltage control loop [36]-[41]. The second approach is based on total energy stored in SM capacitors of a phase leg and difference between energies in upper and lower arms [42]-[45] The third approach is based on open loop control strategy as discussed in [35], [42] and [45].

In the first approach various types of control schemes are investigated. References [36] proposes new averaging and balancing control that controls arm currents as well as reduces circulating currents. Traditional Proportional Integral and Proportional Resonant controllers are presented in [38], [39]. References [40] & [41] provide a deadbeat control approach for faster dynamic response of MMC.

The second approach of energy based control has been investigated for both open loop and closed loop conditions. The open-loop approach [45] is based on estimation of stored energy in the arms by combining the converter voltage references, measured output current and the know DC voltage. In the closed loop approach [43] a decoupled double synchronous frame current control strategy is used to control total leg energy and arm difference energy. The paper uses two rotating frames (for fundamental and 2^{nd} harmonic current) in dq0 co-ordinates to control the total energy oscillations and energy differences.

In order to understand the basic MMC operation a simulation model is developed using a commonly applied control approach. Therefore this section focuses on developing traditional closed loop control system that has been used widely among the literature.

The control system is composed of three control loops. On the top level there is outer power control loop which has two controllers, an active power controller and a reactive power controller. The references for power controllers are defined by the target application. The 2nd level of control loop is the inner phase current control loop. The phase current controller is responsible for producing phase currents of desired amplitude (usually symmetric and sinusoidal). The current controllers are operated in synchronous frame or dq frame domain where three-phase sinusoidal variables are transformed into two-phase DC components using Park transformation. One advantage of this technique is that when these dc components are controlled by proportional-integral controllers, it assures zero steady-state error.

The references for phase current controller are derived from outer power controllers. The output of active power controller is treated as d-axis current controller reference while output of reactive power controller is treated as q-axis current controller reference. Along with the phase current controller another current controller is required, which is the circulating current controller. The circulating current controller is used for minimizing the 2nd harmonic circulating current flowing through phase legs. Outputs of phase current controller and circulating current controller are added together to form complete modulating signal.

The current controller output is called inner emf (e_{j_ref}). Using equations (2.8) and (2.9) the upper and lower arm reference voltages are calculated, where u_{diffj} is the

control voltage generated by circulating current controller. The upper and lower arm reference voltages (u_{pj_ref} and u_{nj_ref}) are biased by Vdc/2, then normalized by dividing with V_{dc} and then passed to the modulation block. The construction and design of all three controllers is discussed in the following section.

PHASE CURRENT CONTROLLER DESIGN:

The goal of phase current controller is to generate modulating signals that produces desired phase currents. The block diagram of a current controller to be designed is shown in Figure 2.9, where Kp, Ki are controller gains, Ts is sampling time, Vdc is DC bus voltage, $R_0 \& L_0$ are resistance and inductance of arm inductor, C_{pk} is carrier frequency peak ($C_{pk} = Vdc$), FSR is full scale range for ADC, G_{TI} is current transducer gain. For simplicity of computation FSR and G_{TI} can be approximated to 1. This makes feedback path gain =1, i.e. unity feedback.

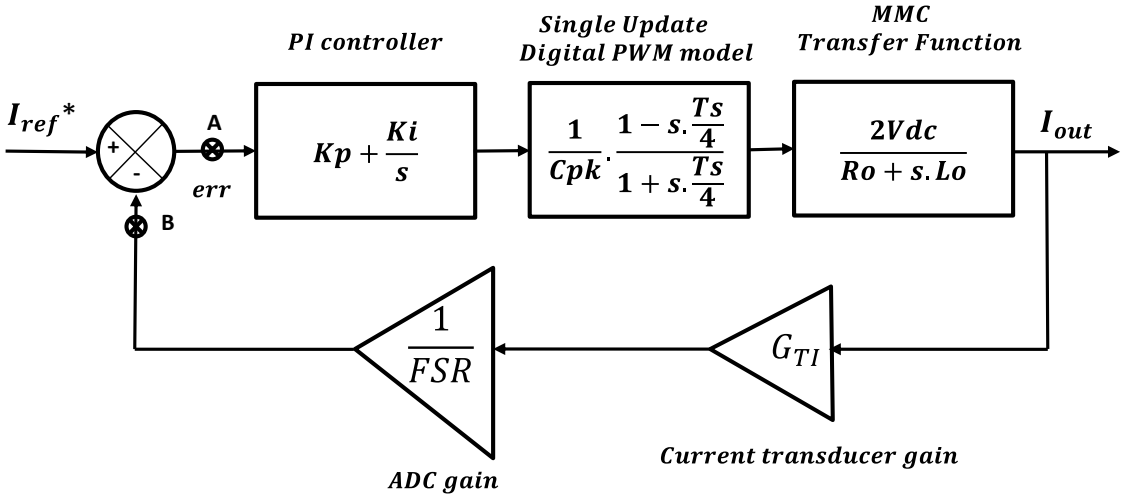

Figure 2.9 Block diagram of phase current control loop

Using block diagram of Figure 2.9 controller gains based on desired gain and phase margins at desired crossover frequency can be calculated. The procedure for calculation of controller gains and bode plots is explained in Appendix A.1.

The closed loop transfer function of complete phase current control loop is given by equation (2.19).

$$G_{CL}(s) = \frac{0.466s^3 + 285.2s^2 + 2.38\text{e}04\ \text{s}}{0.0002626s^4 + 0.5178s^3 + 287.7s^2 + 2.38\text{e}04\ \text{s}} \tag{2.19}$$

The control structure of phase current controllers to be implemented is shown in Figure 2.10. The cross-coupling between d-q axis due to inductance 'Lo' is compensated using feed-forward signals. Decoupling of d-q axis makes the performance of current controller independent of synchronous frame frequency.

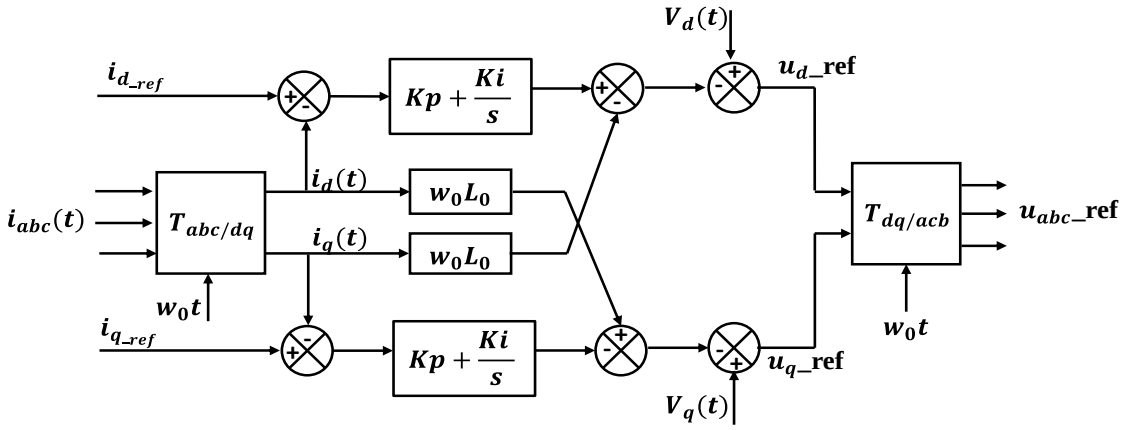

Figure 2.10 Control structure of phase current controllers

ACTIVE AND REACTIVE POWER CONTROLLER DESIGN:

Figure 2.11 and Figure 2.12 shows the block diagram of active and reactive power controllers. Where *Vph* is peak phase voltage and equation (2.19) represents equivalent transfer function of current control loop. By using block diagram of Figure 2.11 and Figure 2.12 controller gains based on desired gain and phase margins at desired crossover

frequency can be calculated. The procedure for calculation of controller gains and corresponding bode plots is explained in Appendix A.2.

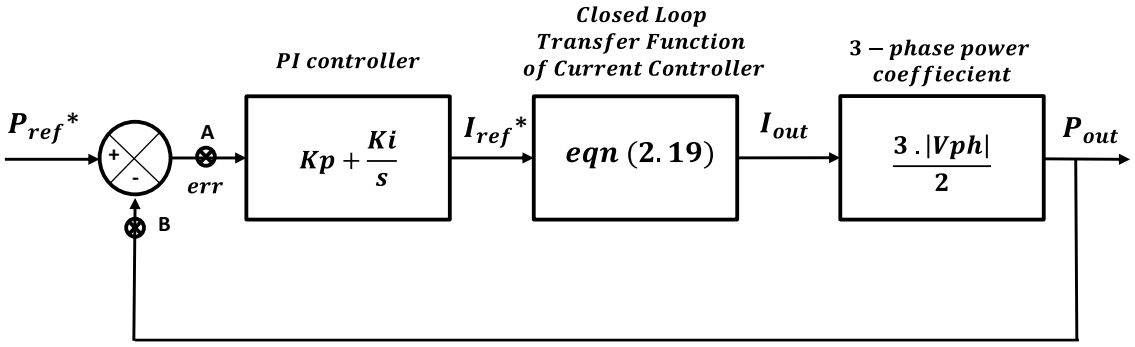

Figure 2.11 Block diagram of Active Power control loop

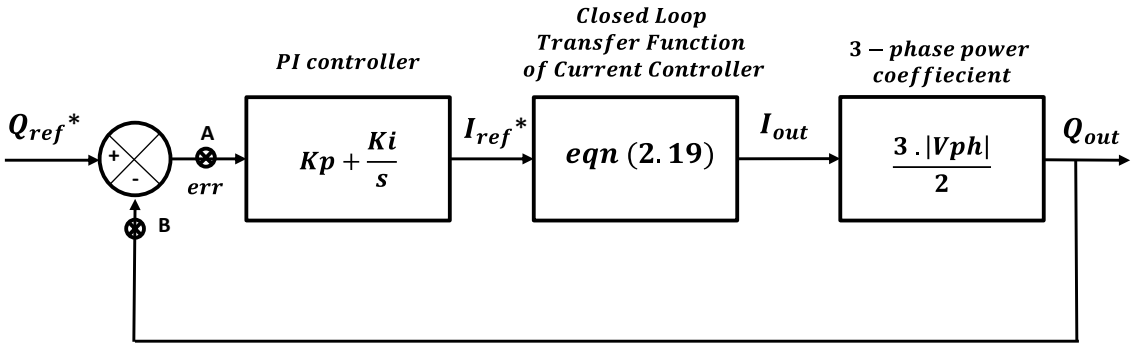

Figure 2.12 Block diagram of Reactive power control loop

The closed loop transfer function of complete power control loop is given by equation (2.20). The control structure of power controllers to be implemented is shown in Figure 2.13.

$$G_{CL}(s) = \frac{0.03812s^7 + 102.6s^6 + 1.002e5\,s^5 + 4.238e7s^4 + 7.736e9s^3 + 6.276e11s^2 + 1.87e13s}{6.896e - 8s^8 + 0.03843s^7 + 103s^6 + 1.005e5s^5 + 4.2448e7s^4 + 7.749e9s^3 + 6.282e11s^2 + 1.875e13s} \quad (2.20)$$

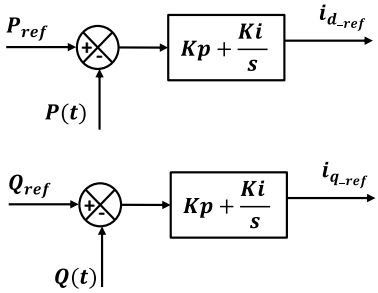

Figure 2.13 Control structure of power controllers

CIRCULATING CURRENT CONTROLLER DESIGN:

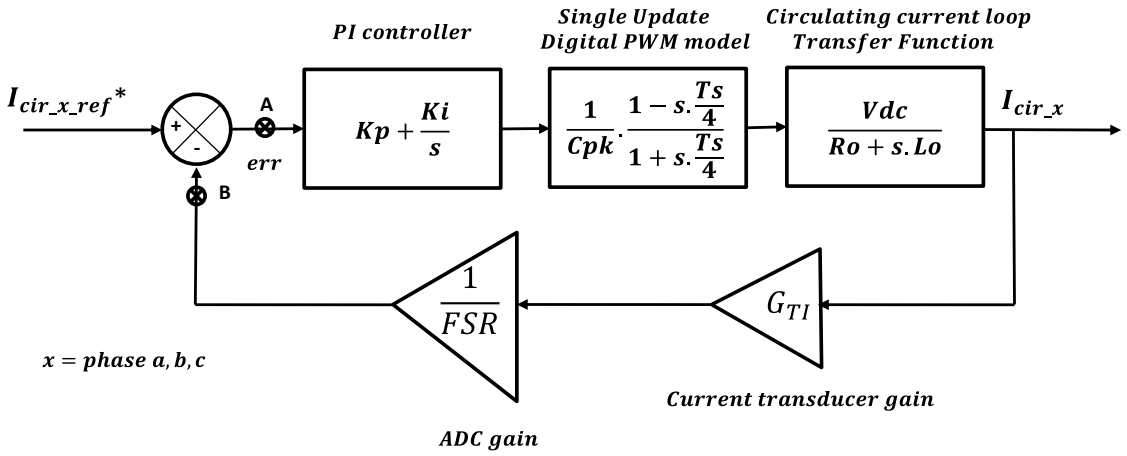

Figure 2.14 Block diagram of circulating current control loop

Figure 2.14 shows block diagram of circulating current control loop. Circulating current controller works in parallel with phase current controller. The goal of circulating current controller is to minimize the 2nd harmonic circulating current within the three phase legs of MMC as requested by its reference input. The reference is usually kept to zero in order to reduce the peak arm currents and losses caused by the circulating current.

By using block diagram of Figure 2.14 controller gains based on desired gain and phase margins at desired crossover frequency can be calculated. The procedure for calculation of controller gains and corresponding bode plots is explained in Appendix A.3. The closed loop transfer function of complete power control loop is given by equation (2.21).

$$G_{CL}(s) = \frac{0.466s^3 + 285.2s^2 + 2.38\text{e}04\ \text{s}}{0.0002626s^4 + 0.5178s^3 + 287.7s^2 + 2.38\text{e}04\ \text{s}} \tag{2.21}$$

Figure 2.15 shows the control structure of the circulating current suppressing controller [10]. The circulating current of each phase is calculated by adding respective

upper and lower arm currents and then dividing by 2 according to equation (2.3). This three-phase current is then transformed into the double line frequency negative sequence rotational frame (i_{2fd} & i_{2fq}). The references for d and q axis controllers are zero since circulating current should not have any AC components. The controller outputs are then transformed back to three-phases using inverse park transformation $T_{dq/acb}$.

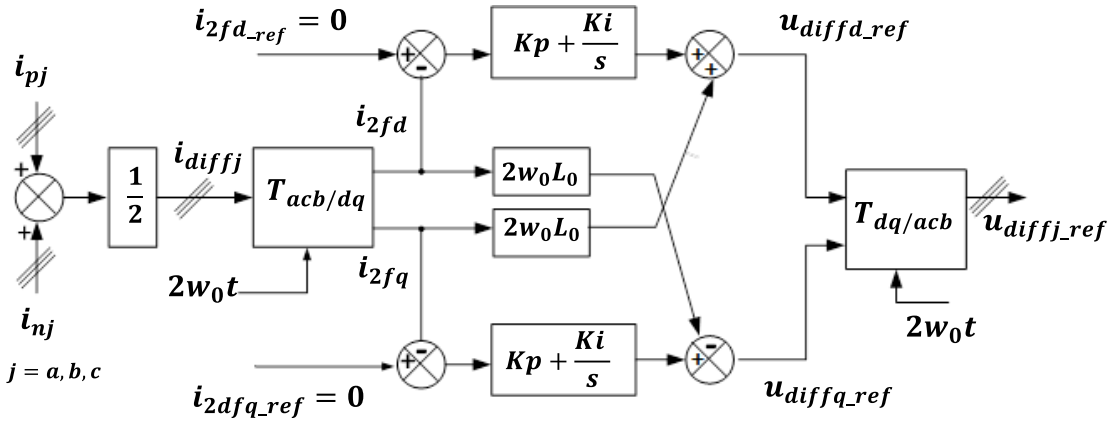

Figure 2.15 Control structure for circulating current controller

2.5 SIMULATION VERIFICATION OF MMC SYSTEM WITH DESIGNED CONTROLLERS

In order to verify the operation of PSC-PWM modulation method, conventional voltage balancing algorithm and all the controllers a simulation model was developed. Figure 2.16 shows the system connections used for MMC simulation where the MMC from Figure 2.1 is implemented. The simulation is carried out for a six-level MMC that is connected between AC grid and a DC bus. The simulation was performed in Simulink.

Table 2.1 lists circuit parameters and operating conditions used for the test MMC. The MMC is designed for full load rated power of 60kVA.

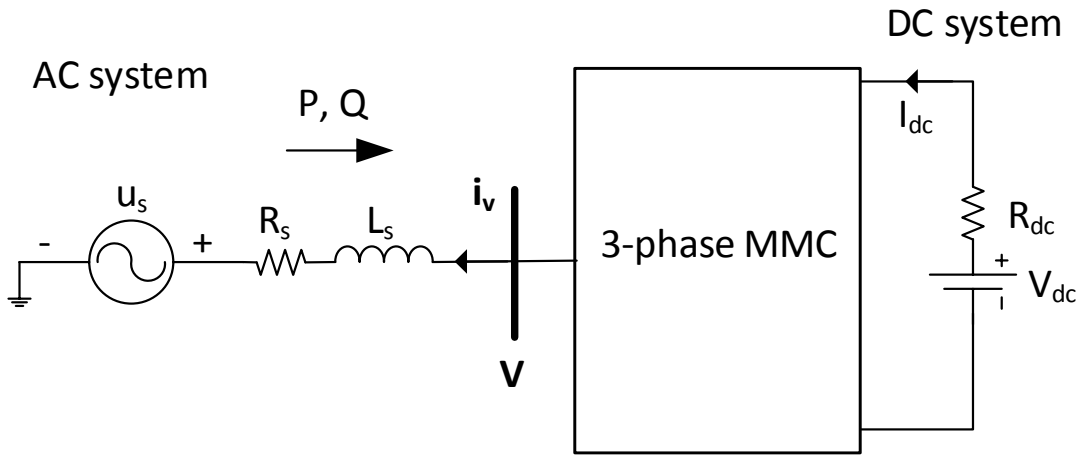

Figure 2.16 Simulation system connections between AC and DC bus

Table 2.1 Main Circuit Parameters and Operating Conditions of Simulated System

Parameters	Designation	Values
Active power	P	60kW
Reactive power	Q	20kVar
Ph-Ph RMS AC voltage	Vg	208V
AC system inductance	Ls	0.1nH
AC system Resistance	Rs	0.1Ohm
DC bus voltage	Vdc	800V
DC resistance	Rdc	0.01Ohm
Number of SM per arm	N	6
SM capacitance	Co	15000uF
Arm Inductance	Lo	1mH
Arm equivalent resistance	Ro	0.1Ohm
SM capacitor voltage	Vc	133.33V
Carrier frequency	Fc	500Hz
Sampling frequency	Fs	3000Hz

Some of the important results of simulation are shown in Figure 2.17. The simulation begins with P=30kW and Q=0Var as shown Figure 2.17 (a). The step change in active and reactive power occurs at 0.2sec with P=60kW and Q=20kVar. Both the active and reactive power reach to steady state within 0.1sec. Phase currents are sinusoidal and symmetric (Figure 2.17 (c)). Circulating currents are minimized to a small value after CCSC is enabled at 0.15sec (Figure 2.17 (e)). This validates the performance of all the controllers.

The performance of circulating current suppressing controller (CCSC) is also shown in Figure 2.18. Prior to enabling this controller the circulating current is about 12A peak to peak and after enabling the controller it minimized to about 3A peak to peak. Also it can be observed from Figure 2.17 that the circulating current controller doesn't affect the operation of other controllers and other system parameters. The performance of the conventional voltage balancing algorithm is shown in Figure 2.19. All the six capacitor voltages in one arm have very similar voltage waveform. This indicates excellence voltage balancing among all the capacitors in one arm.

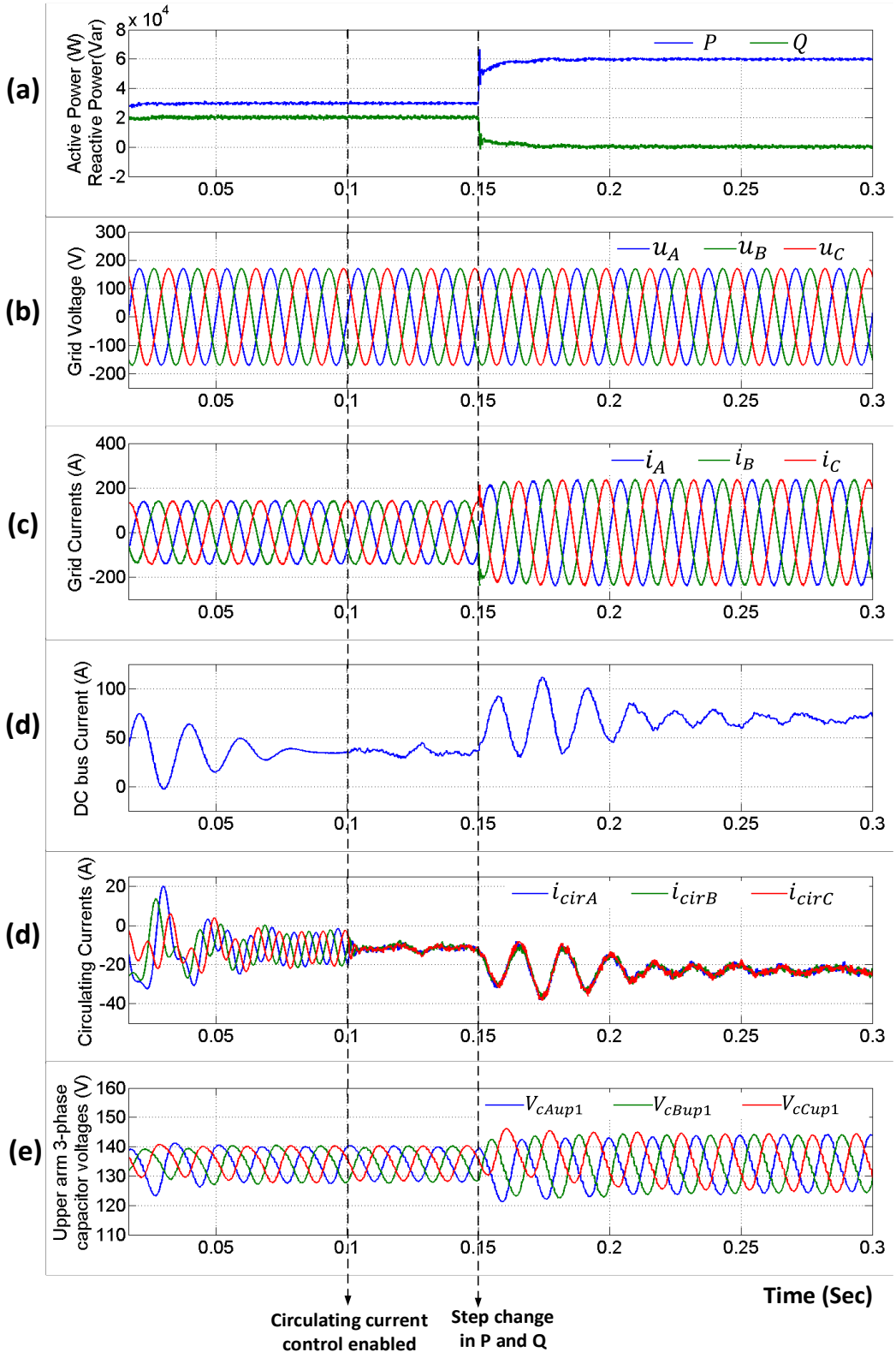

Figure 2.17 Simulation results (a) Active and Reactive powers (b) Grid voltages (c) Grid currents (d) DC current (e) Circulating current (f) Upper arm three-phase capacitor voltages

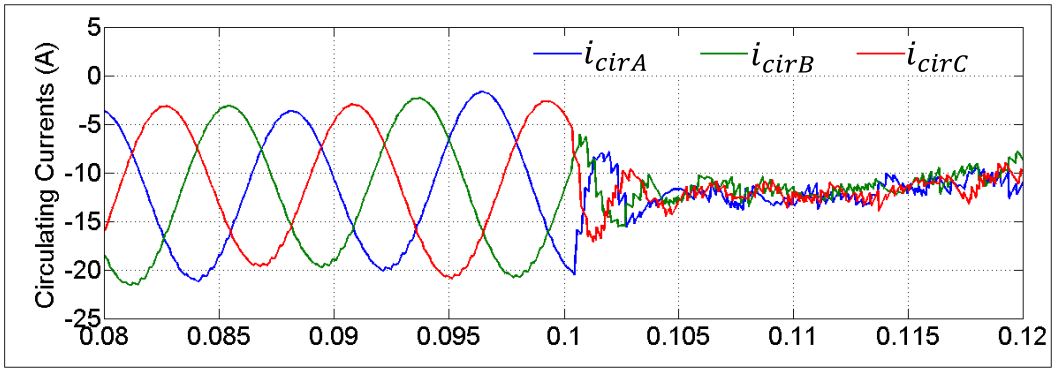

Figure 2.18 Performance of circulating current controller (enabled at 0.15sec)

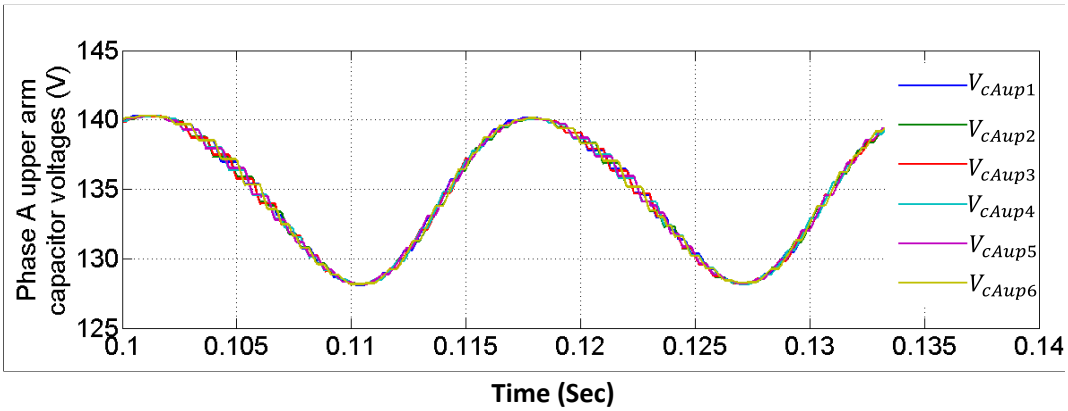

Figure 2.19 Performance of conventional voltage balancing method

This chapter discussed some fundamentals of modular multilevel converter and control design. Time-domain modeling of MMC, multilevel modulation schemes and conventional voltage balancing algorithm was briefly presented. Also, active/reactive power, phase current and circulating current control methods for MMC were developed using PI controllers and theoretical design was confirmed using bode plots and Nyquist criteria. The complete three-phase MMC system was tested in simulation and results were obtained that show the MMC performs acceptably under balance grid voltage conditions.

CHAPTER 3

MODULAR MULTILEVEL CONVERTER WITH NON-IDEAL AC SUPPLY

This chapter discusses the performance of the traditional control system for MMC under non-ideal AC supply condition. A set of fault test cases is created to observe the controller performance and its effect on various system parameters.

3.1 MMC PERFORMANCE UNDER NON-IDEAL GRID CONDITIONS

Various types of modulation schemes, voltage balancing algorithms, circulating current reduction techniques and harmonic minimization schemes that control the MMC under normal operating conditions have been proposed.. But the operation of a MMC under asymmetric or non-ideal grid supply voltage conditions is still under developed and needs more investigation in order to obtain the best possible performance under those conditions.

Using the MMC model described in Chapter 2, a system simulation was carried out to study the MMC's performance under asymmetric grid supply voltage conditions. In this simulation test case, grid phase-A voltage is reduced from 1.0 pu to 0.01 pu during normal steady-state operation of the converter to represent a single phase to ground fault

as shown in Figure 3.1 where term VU on the top is abbreviation for "Voltage Unbalance"

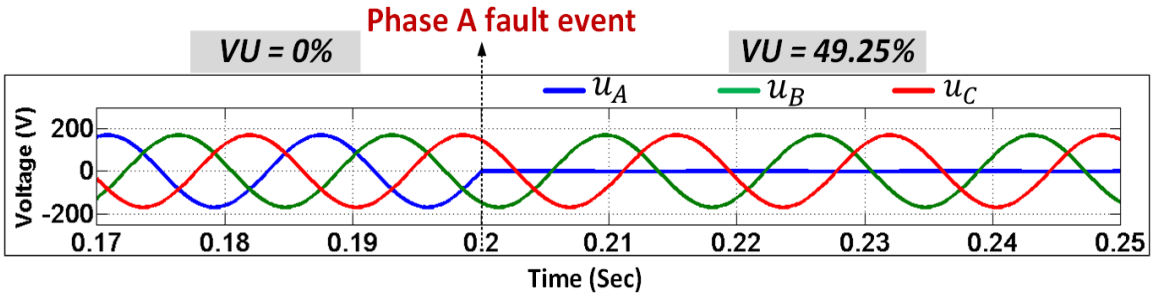

Figure 3.1 Grid voltage unbalance test-case for simulation

Using Fortescue transformation (explained in Appendix A) the symmetric component decomposition of corresponding three-phase voltages is shown in Table 3.1.

Table 3.1 Symmetric component decomposition of unbalanced grid voltages test case

Parameter	Voltages: mag(pu)∠(deg)
Grid unbalance test case	V_A = 0.01∠ 0deg V_B =1∠-120deg V_C = 1∠ 120deg
Positive sequence component	V^+ = 0.67∠ 0deg
Negative sequence component	V^- = 0.33∠ 180deg
Zero sequence component	V^0 = 0.33∠ 180deg
Voltage Unbalance (VU) 100*(Negative seq. Volt / Positive seq. Volt)	49.25%

The simulation results are shown in Figure 3.2, Figure 3.3 and Figure 3.4. Figure 3.2 shows the effect of unbalance supply voltage on the corresponding d-q axis voltage and

current controller reference components. Due to unbalance voltages a 2nd harmonic sinusoidal component appears in both d and q axis grid voltage components. This affects operation of active and reactive power controllers. The power controllers then produce d-q axis current references which are also affected by the 2nd harmonic ripples. The references produced by phase current controller and circulating current controllers are shown in Figure 3.3.

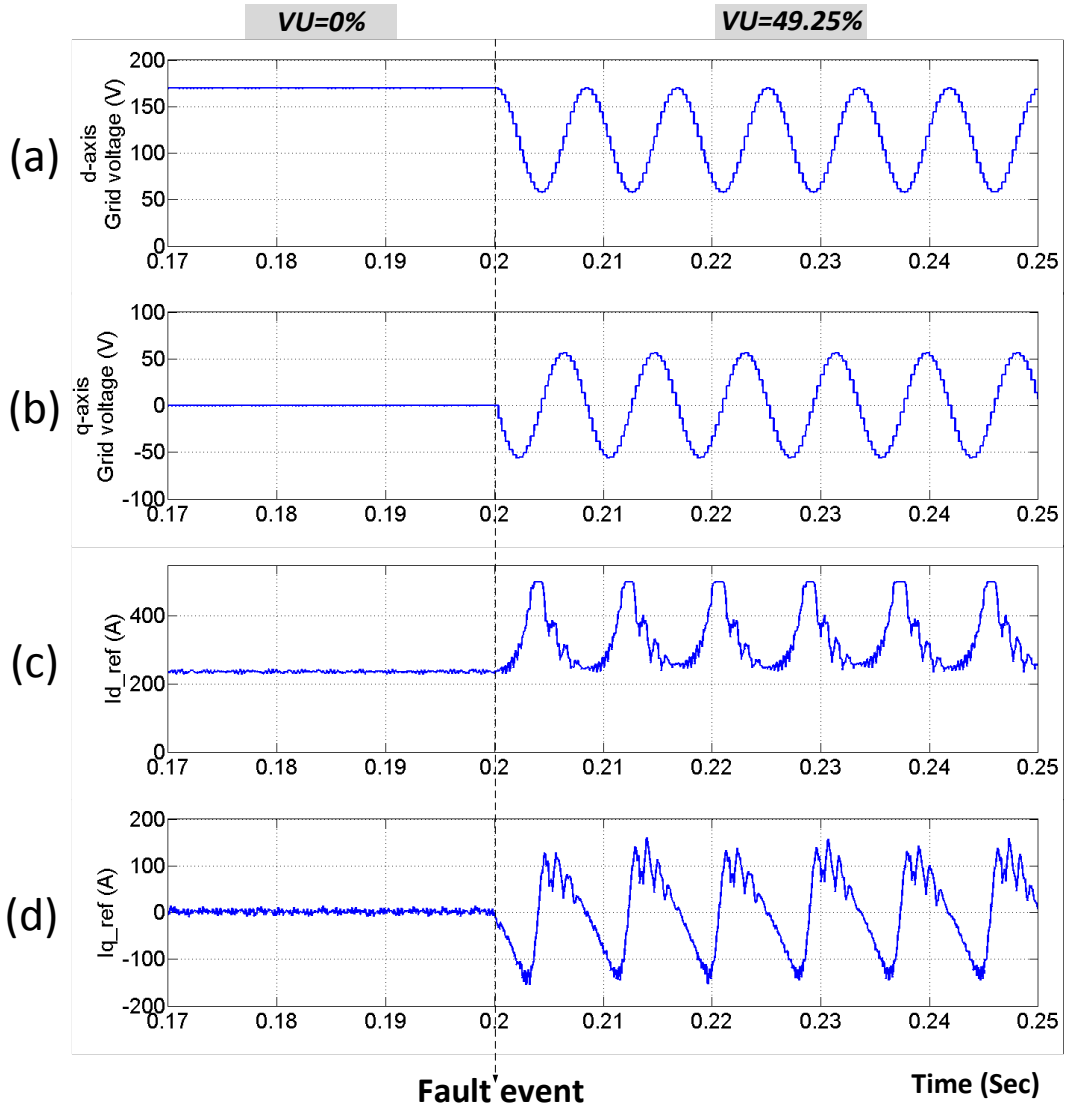

Figure 3.2 Various d-q axis components (a) d-axis grid voltage (b) q-axis grid voltage (c) d-axis phase current controller reference generated by active power controller (d) q-axis phase current controller reference generated by reactive power controller

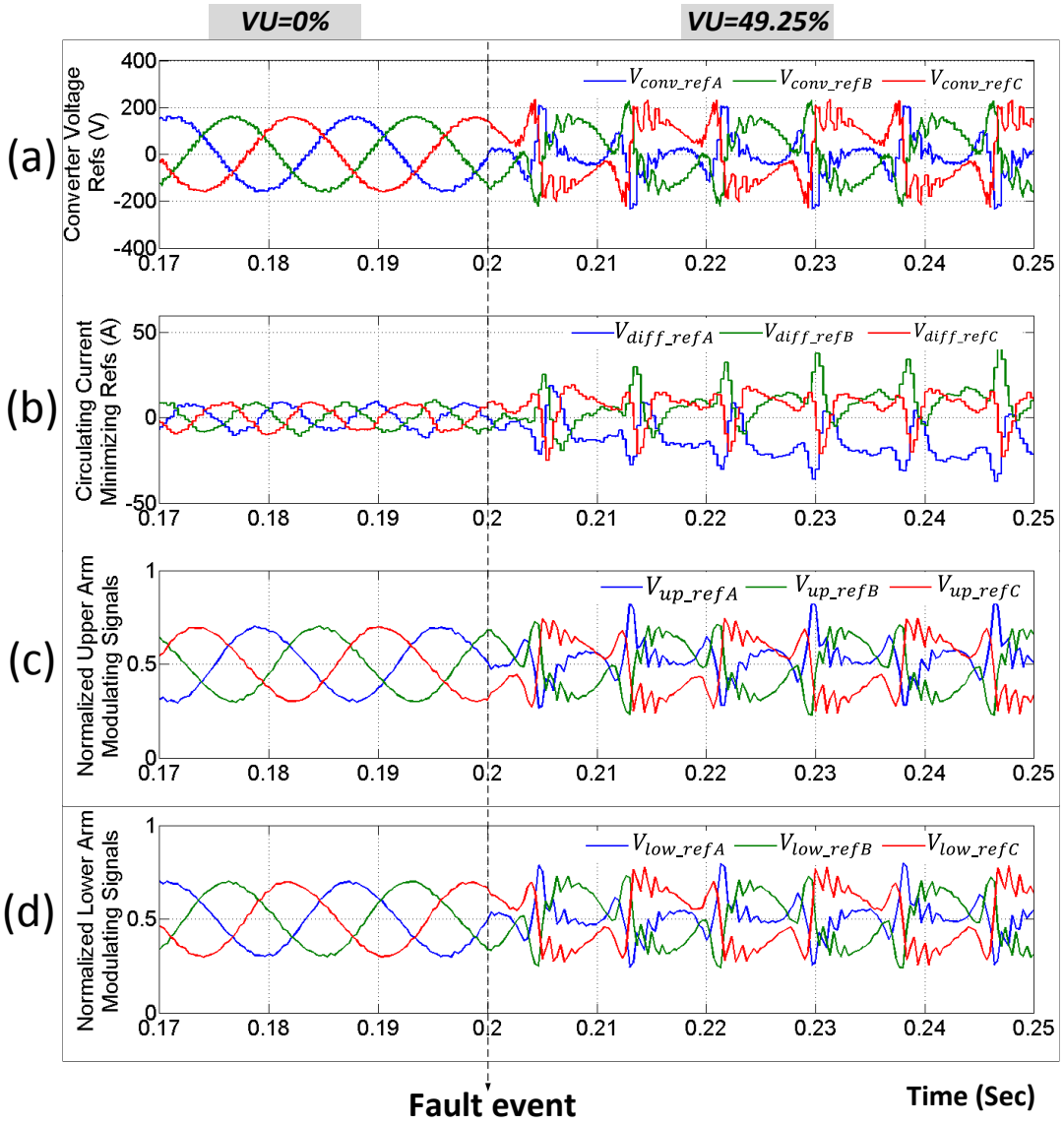

Figure 3.3 Various reference signals (a) Converter voltage modulating signal generated by phase current controllers (b) Circulating current modulating signal generated by circulating current controllers (c) Upper arm complete normalized modulating signal (d) Lower arm complete normalized modulating signal

From Figure 3.2 and Figure 3.3 it is clear that the modulating signals are non-sinusoidal which will result in non-sinusoidal phase currents. This also affects other system parameters such as capacitor voltages, circulating currents and dc bus current. Figure 3.4 illustrates the effect of unbalance voltages on these quantities.

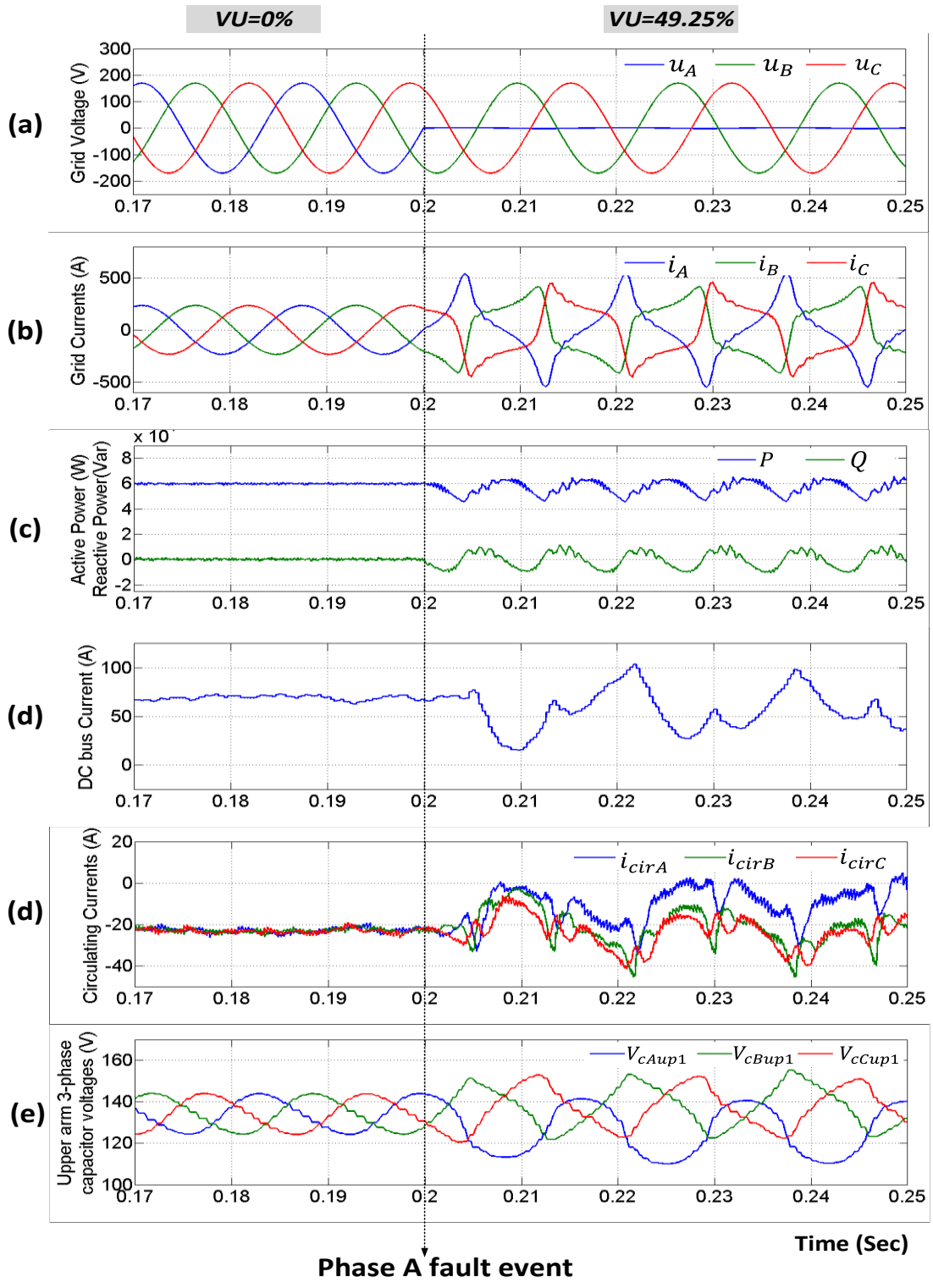

Figure 3.4 Performance of traditional MMC control scheme under unbalance supply voltage (a) Grid voltages (b) Grid currents (C) Active and Reactive powers (d) DC current (e) Circulating current (f) Upper arm three-phase capacitor voltages

As expected from the modulating signals the phase currents are non-sinusoidal also their peak magnitude is approximately twice higher as compared to the symmetrical supply condition. A converter designed for rated power during balance supply condition may not be able to withstand such a high peak currents. Using FFT analysis the frequency components in the phase currents are obtained as shown in Figure 3.5. It can be seen that 3^{rd}, 5^{th} and 7^{th} harmonics are dominant in converter supply currents.

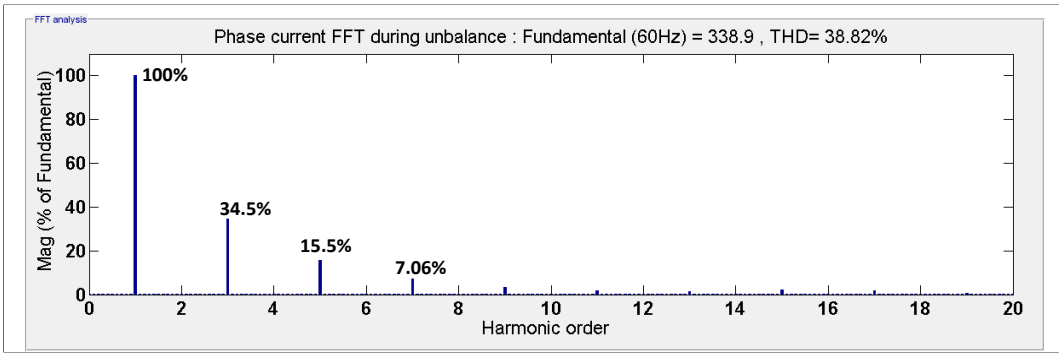

Figure 3.5 Frequency spectrum of phase currents during unbalance condition

Due to the non-sinusoidal nature of phase currents the sub-module capacitors also have non-sinusoidal voltage ripple. These non-sinusoidal voltage ripples then cause non-sinusoidal circulating currents which make it impossible to minimize them using the controller shown in Figure 2.15 since the circulating current controller operates in 2^{nd} harmonic synchronous frame. A frequency spectrum of circulating current during unbalance is shown in Figure 3.6.

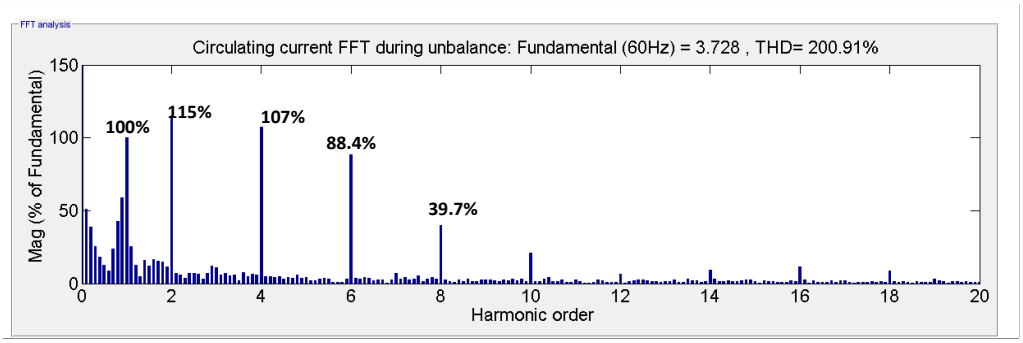

Figure 3.6 Circulating current frequency spectrum during unbalance

From Figure 3.6 it is noted that due to the nature of capacitor voltage unbalance only even harmonic components are present in the circulating currents.

Active and reactive powers (Figure 3.4 (c)) have large ripples during fault. Due to the ripples in active power and harmonics in circulating currents the dc bus current also has ripples as shown in Figure 3.4 (d). This causes significant ripples in the dc power as well.

From the results discussed above it is clear that the traditional control approach fails to maintain acceptable performance of a MMC under unbalance conditions. It is therefore necessary to investigate the recent development in this area and understand what new strategies have been proposed and validated to improve MMC performance during asymmetrical supply conditions.

3.2 PREVIOUSLY SUGGESTED METHODS FOR MMC PERFORMANCE IMPROVEMENT UNDER SUPPLY ASYMMETRY

There has been some initiative taken by various researcher [46], [47], [48], [49], [50], [51], [52], [53] and [54] to address performance improvement under asymmetrical supply conditions. Reference [48], [50], [52], [53] & [54] proposes control reference calculation methods based on decomposition of symmetric components into positive, negative and zero sequence components in d-q frame of reference. All of these methods still suffer from various issues such as large fault transient in phase currents, higher steady state peak value of phase current, ripples in active and reactive powers, higher voltage ripple on sub-module capacitors etc.

Reference [49] attempts to remove dc bus voltage ripple by injecting zero sequence control reference into the modulating signal based on six arm inserted voltages but it to has ripples in active and reactive powers and higher magnitude of phase currents during fault. Reference [38] proposes stationary frame based proportional-resonant controller but has similar issues as mentioned above. Therefore, the need for further improvement in performance of MMCs under non-ideal grid supply conditions resulted in the method described in Chapter 4 which addresses the shortcomings outlined above.

CHAPTER 4

ADVANCED CONTROL STRATEGY FOR MODULAR MULTILEVEL CONVERTERS UNDER NON-IDEAL SUPPLY CONDITIONS

In order to properly control a MMC under the more general conditions of asymmetrical supply voltage an appropriate framework is needed. To manage the unbalanced currents in the converter under such conditions an orthogonal decomposition of the current that separates the unbalanced portion and balanced portions can be used. The following sections describe development of a new MMC control structure based on an appropriate current decomposition.

4.1 CURRENT'S PHYSICAL COMPONENT (CPC) POWER THEORY

The CPC theory was developed in the frequency domain by Czarnecki [46] is based on orthogonal decomposition of the current. This theory provides a physical interpretation of power phenomena in three-phase systems under unbalanced and non-sinusoidal conditions.

The theory decomposes the current into active, reactive, unbalanced and harmonic components.

$$i = i_a + i_r + i_u + i_h \tag{4.1}$$

where, i is defined as a vector of three phase currents $[i_A\ i_B\ i_C]^T$ and i_a, i_r, i_u, i_h, are defined as active, reactive, unbalanced and harmonic components of that current vector respectively. In a power converter system fed with sinusoidal supply voltages, only the active power, reactive power and unbalanced power of the fundamental are concerned, and it is not necessary to decompose all the harmonics. Then, a subset of the theory, namely, the fundamental current component is expressed as follows:

$$i = i_a + i_r + i_u \tag{4.2}$$

Consider Figure 4.1 (a) which shows a linear, time-invariant load supplied with a sinusoidal symmetrical voltage of positive sequence and consumes only active power. For any such system there exists an equivalent resistive and balanced load, shown in Figure 4.1 (b), which has same voltage and the same active power P as the original load. Similarly, there can be representation of a three phase system that only provides reactive power as shown in Figure 4.2 (a). The equivalent representation of such system would be an inductive and balanced load as shown in Figure 4.2 (b).

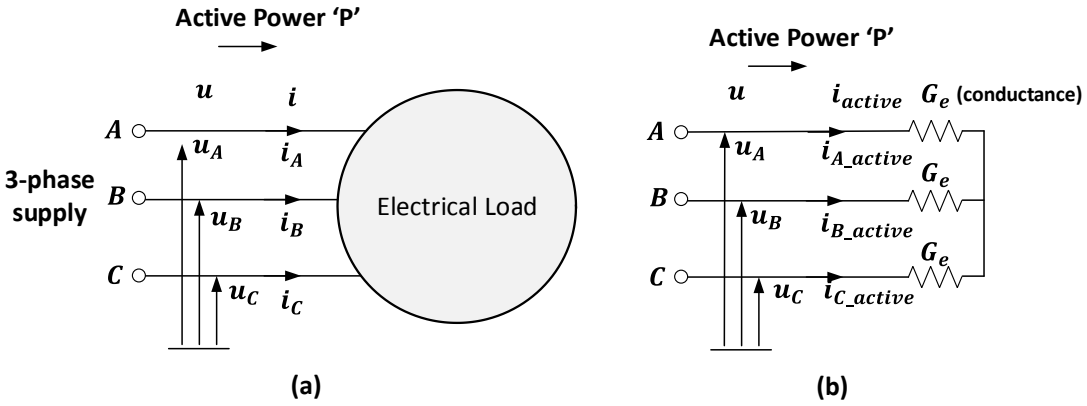

Figure 4.1 Three phase system with active power

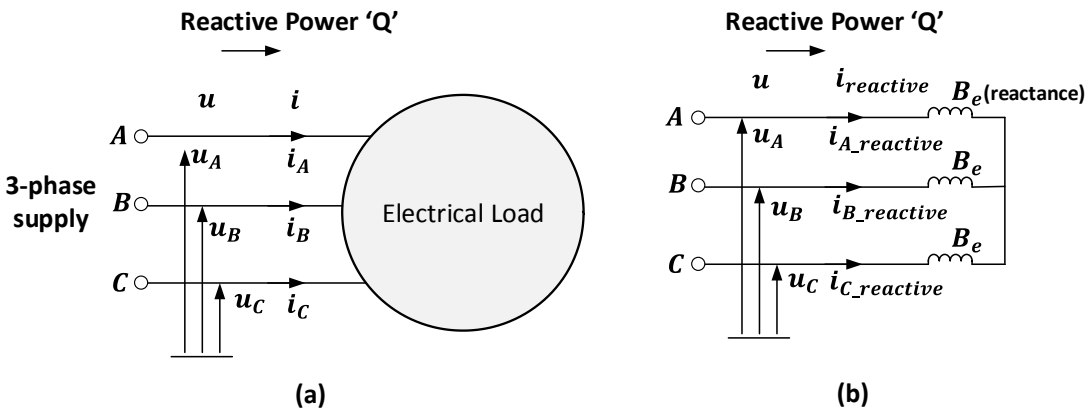

Figure 4.2 Three-Phase system with reactive power

The case where the three-phase system has to supply both active and reactive powers can be represented by equivalent admittance load as shown in Figure 4.3.

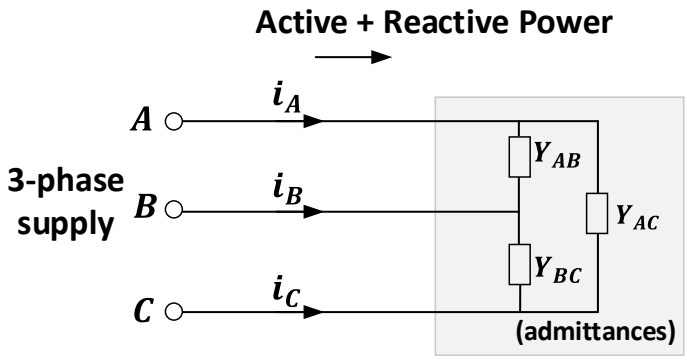

Figure 4.3 Three-Phase system equivalent circuit with both active and reactive powers

Under balanced supply and balanced load conditions the system of Figure 4.3 only consists of active and reactive powers. But if either of the supply or load is unbalanced then along with active and reactive powers there will exist a third component called unbalanced power. These powers are directly related to active, reactive and unbalanced currents. These currents are orthogonal. For converter control purposes these current components need to be decomposed so that they can be controlled individually. In order to perform this decomposition the load is expressed in terms of two admittances the

equivalent admittance and the unbalanced admittance. The equivalent admittance is expressed as

$$Y_e = G_e + jB_e = Y_{AB} + Y_{BC} + Y_{AC} \tag{4.3}$$

Where, G_e & B_e are the equivalent conductance and equivalent susceptance respectively. The unbalanced admittance is

$$A = Ae^{j\emptyset} = Acos\emptyset + jAsin\emptyset = (Y_{AB} + \alpha Y_{BC} + \alpha^* Y_{AC}) \tag{4.4}$$

where, $\boldsymbol{\alpha} = e^{j120^0}$ and $\boldsymbol{\alpha}^* = e^{-j120^0}$.

During symmetrical supply conditions there is only a positive sequence voltage component present in the system. But during asymmetrical supply conditions, the supply consists of positive, negative as well as zero sequence voltage components. In this situation a decision must be made regarding what sort of power should be consumed. Consuming power with respect to the negative sequence voltage component means injecting negative sequence current in to the grid. This is generally not feasible since many circuit breakers are designed to detect negative sequence current components and trip the breaker. Consuming power from zero sequence voltage components means injecting zero sequence current into the grid. Zero sequence power never exists with only dc value or only ripple, rather it has both dc and ripple components. Therefore the power ripple is unavoidable if zero sequence power is consumed. In addition, the zero sequence current also causes many other issues such as high neutral current, high neutral to ground voltage, low power factor, high system losses etc. Therefore the only way a good quality of power that can be consumed during unbalanced voltage is by using positive sequence voltage component.

Using the positive sequence voltage component it is possible to inject amplitude and phase symmetric positive sequence currents into the grid producing power components that are ripple free. If the phase currents are balanced then the circulating currents can also be controlled. This also would result in ripple free power on the dc side as well. Due to these reasons for the developed MMC control method presented later the decomposition of phase currents into active, reactive and unbalance components is done with respect to positive sequence supply voltage.

Having the admittances from equation (4.3) and (4.4) the three-phase active current vector can now be written as a function of positive sequence supply voltage as given by,

$$\boldsymbol{i_a} = \sqrt{2}Re\left\{Ge\left[\boldsymbol{U_A}^+ \ \boldsymbol{U_B}^+ \ \boldsymbol{U_C}^+\right]^T e^{jw_1 t}\right\} \tag{4.5}$$

The voltages $\boldsymbol{U_A}, \boldsymbol{U_B}$ & $\boldsymbol{U_C}$ are symmetrical since they are positive sequence components, then above equation becomes,

$$\left[\boldsymbol{U_A}^+ \ \boldsymbol{U_B}^+ \ \boldsymbol{U_C}^+\right]^T = \left[\boldsymbol{U}^+ \ \ \boldsymbol{U}^+\boldsymbol{e}^{-j2\pi/3} \ \ \boldsymbol{U}^+\boldsymbol{e}^{j2\pi/3}\right] \tag{4.6}$$

Then

$$\boldsymbol{i_a} = \begin{bmatrix} i_{Aa} \\ i_{Ba} \\ i_{Ca} \end{bmatrix} = \sqrt{2}Ge \begin{bmatrix} \boldsymbol{U}^+cos(wt) \\ \boldsymbol{U}^+cos(wt - 2\pi/3) \\ \boldsymbol{U}^+cos(wt + 2\pi/3) \end{bmatrix} \tag{4.7}$$

Similarly,

$$\boldsymbol{i_r} = \sqrt{2}Re\left\{jBe\left[\boldsymbol{U_A}^+ \ \boldsymbol{U_B}^+ \ \boldsymbol{U_C}^+\right]^T e^{jw_1 t}\right\} \tag{4.8}$$

$$\boldsymbol{i_r} = \begin{bmatrix} i_{Ar} \\ i_{Br} \\ i_{Cr} \end{bmatrix} = \sqrt{2}Be \begin{bmatrix} \boldsymbol{U}^{+} sin(wt) \\ \boldsymbol{U}^{+} sin(wt - 2\pi/3) \\ \boldsymbol{U}^{+} sin(wt + 2\pi/3) \end{bmatrix} \tag{4.9}$$

And

$$\boldsymbol{i_u} = \sqrt{2}Re\left\{A\left[\boldsymbol{U_A}^{+} \;\; \boldsymbol{U_B}^{+} \;\; \boldsymbol{U_C}^{+}\right]^{T} e^{jw_1 t}\right\} \tag{4.10}$$

$$\boldsymbol{i_u} = \begin{bmatrix} i_{Au} \\ i_{Bu} \\ i_{Cu} \end{bmatrix} = \sqrt{2}A \begin{bmatrix} \boldsymbol{U}^{+} cos(wt + \emptyset) \\ \boldsymbol{U}^{+} cos(wt + \emptyset + 2\pi/3) \\ \boldsymbol{U}^{+} cos(wt + \emptyset - 2\pi/3) \end{bmatrix} \tag{4.11}$$

By extracting frequency domain components of grid voltages and phase currents (as explained in next section) active, reactive and unbalance current components present in the phase currents can be found. Then by using the above mentioned relationship between grid voltages, currents and system admittances the desired phase current references can be generated. These references can then be used to control the phase currents using proportional–resonant controllers operating in the ABC frame in order to control them individually.

4.1.1 RDFT BASED HARMONIC COMPONENT EXTRACTION

During unbalance supply conditions in order to extract desired frequency and symmetric components of supply voltage some methodology is required. Traditional techniques use digital filters in order to extract the desired components of voltage or current. Unfortunately, even for low-order filters, these methods may require longer times than two cycles of the fundamental in order to reach steady state after the occurrence of a

transient. In order to improve the performance of the reference current generation while preserving the computational efficiency, a reference generation technique for active compensators based on the use of a computationally efficient Recursive Discrete Fourier transform (RDFT) was presented in [55]. The proposed strategy utilizes the RDFT instead of the filters typically used to extract the desired components of the voltage or current. Using this technique it is possible to extract the fundamental component of grid voltages and also decompose the symmetric components of fundamental voltages as will be shown later in this chapter (section 4.3). The derivation of RDFT method is explained below.

Assuming that at sample k a time window comprises the N values (or samples)

$$\{x(k\text{-}N\text{+}1),\ x(k\text{-}N\text{+}2),\ \ldots.,\ x(k)\}$$

The complex RMS (CRMS) value of the fundamental harmonic is given by the DFT as

$$\tilde{\mathbf{X}}_1(k) = \tilde{\mathbf{X}}_1(k-1) + \frac{\sqrt{2}}{N}(x(k) - x(k-N))[\cos\omega_{1g}k - j\sin\omega_{1g}k] \tag{4.12}$$

Where, ω_{1g} is a fixed fundamental frequency of the grid voltage that defines the sampling period and sampling numbers N in one power period. Further, the real and imaginary terms of the signal can be separated as shown in equation (4.13)

$$\begin{aligned}\tilde{\mathbf{X}}_1(k) &= \mathrm{Re}\{\tilde{\mathbf{X}}_1(k)\} + j\,\mathrm{Im}\{\tilde{\mathbf{X}}_1(k)\} \\ &= [\mathrm{Re}\{\tilde{\mathbf{X}}_1(k-1)\} + \frac{\sqrt{2}}{N}(x(k) - x(k-N))\cos\omega_{1g}k \\ &\quad + j[\mathrm{Im}\{\tilde{\mathbf{X}}_1(k-1)\} - \frac{\sqrt{2}}{N}(x(k) - x(k-N))\sin\omega_{1g}k]\end{aligned} \tag{4.13}$$

This method can be seen as a normal DFT in a sliding window but with the reduced calculations. This technique is used here in order to extract desired frequency

components of voltages and also for decomposing fundamental signal into positive, negative and zero sequence symmetric components. The design of MMC control system based on CPC power theory and using RDFT algorithm is discussed in the following section.

4.2 CPC BASED CONTROL STRUCTURE DESIGN

A control system for MMC based on CPC theory is similar to the traditional control system designed in chapter 2 that is, active & reactive power controllers, phase current controllers and circulating current controller. It is important to note that the DC bus voltage controller is not needed for MMC since the modulation technique inherently keeps the DC bus voltage constant by maintaining fixed number of sub-module capacitors across the phase legs. Therefore the only variable on the dc side is the DC current, which is indirectly controlled by the active power controller and circulating current controller. During balance supply only active power controller indirectly controls the dc bus current but during unbalance supply the performance of circulating current controller also decides the magnitude of ripples in the dc bus current.

The key differences between control system designed in chapter 2 and CPC based control system is that the CPC based control system uses only positive sequence component of grid supply voltage to produce desired active and reactive powers and also the CPC based phase current controllers and circulating current controllers work in ABC frame to have individual control of each phase current.

Figure 4.4 shows the simplified block diagram of CPC based complete control structure for MMC system. The entire control system has three different types of

controllers, active/reactive power controllers, phase current controllers and circulating current controllers.

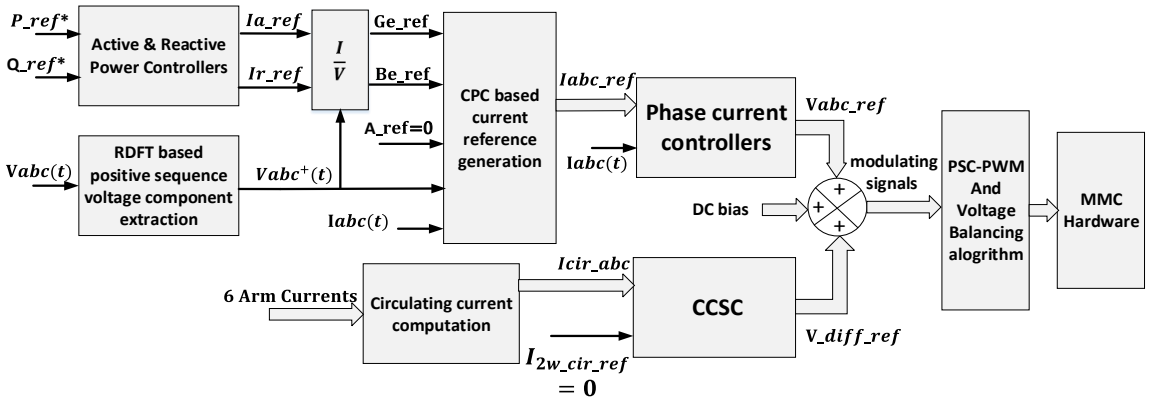

Figure 4.4 Complete CPC based control structure for MMC

The power controller generates active and reactive power current references. These references are divided by magnitude of positive sequence voltage component which yields equivalent conductance and reactance references. The positive sequence voltage components are obtained by using RDFT based algorithm. Then using equivalent admittance, reactance, phase currents and positive sequence voltages phase current references are computed using CPC based calculations. The phase current controllers generate part of the modulating signal based on current references. The other part of the modulating signal is generated by circulating current controllers.

The circulating current references are fixed to zero and instantaneous circulating currents are computed by using the arm current measurements (equation (2.3)). The sinusoidal component of circulating current is minimized by injecting the opposite phase harmonic in the arm currents. Important thing to note here is that the control input from phase current controllers is ‘added’ in upper arm modulation and ‘subtracted’ from lower arm modulation block. This is required to create 180 deg phase shift (ideally) between upper arm and lower arm currents. This phase shift is needed to create sinusoidal shaped

AC staircase voltage at the virtual midpoint of MMC phase legs. But on the other hand since the circulating current only flows in the phase legs the only way to minimize it is to "add" control input to both upper and lower arm modulations. This would create a component of 2nd harmonic and opposite phase (180deg shifted) into phase legs which would cancel the effect the original circulating current component and hence minimize it.

The detail design procedure for CPC based control system and validation of all control subsystems will be discussed in subsequent sections.

4.2.1 Phase Current Controller Design

The goal of the phase current controller is to be able generate sinusoidal currents with peak magnitude as defined by its reference (coming from active/reactive power controllers). As explained in chapter 2, traditionally the phase current controller is designed either in $\alpha - \beta$ domain using Clark transformation or in $d - q$ domain using Park transformation to assure zero steady state error by using PI controllers. This method gives good performance during balance supply condition. But during unbalance supply the existence of negative sequence, zero sequence and possibly harmonics in the supply voltage affects the operation of these controllers and they fail to produce desired results such as symmetric sinusoidal currents and ripple free active and reactive and DC powers. Therefore a Proportional –Resonant (PR) controller is designed in ABC frame which also assures zero steady state error and the references for these PR controllers are directly available from CPC based current reference generation algorithm as shown in Figure 4.4

A current control loop block diagram with Proportional-Resonant controller is shown in Figure 4.5. The block diagram is very similar to Figure 2.4 except that it has

proportional resonant controller and the inputs are individual phase currents so there will be three proportional-resonant current controllers for the three phase system.

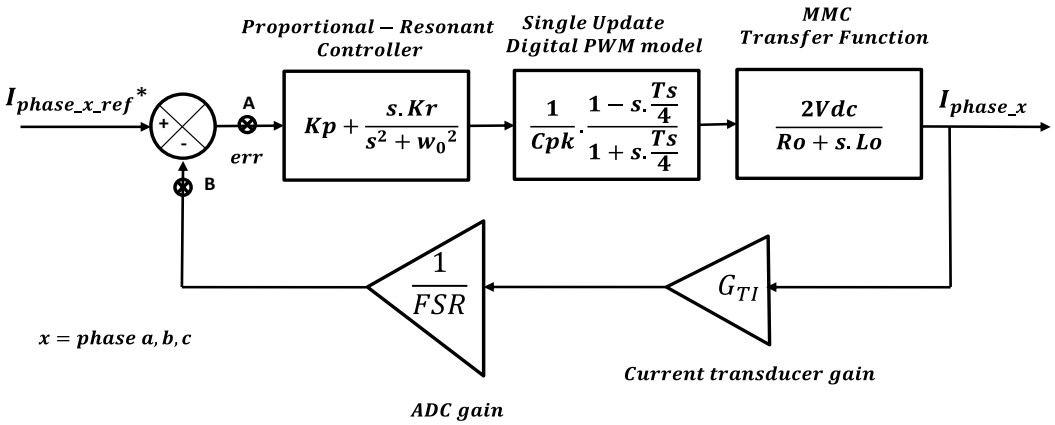

Figure 4.5 CPC based current control loop block diagram

The proportional resonant controller is tuned to fundamental frequency of the phase current to be controlled. In this case it is same as grid supply voltage frequency. The design of proportional-resonant controller is not as simple as PI controller as it was done in chapter 2 due to existence of 2nd order polynomial terms in controller transfer function. Therefore a different approach is taken to compute the controller gains. This method is called as Naslin polynomial matching technique [54]. Naslin polynomial matching technique can be used to find proportional and resonant gains by matching system's closed loop characteristic polynomial with Naslin polynomial and then solving for relevant coefficients. The derivation of controller gains using Naslin polynomial technique is explained in Appendix B.1.

From Appendix B.1 the closed transfer function is obtained as,

$$G_{CL}(s) = \frac{a_7 s^7 + a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_8 s^8 + b_7 s^7 + b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{4.14}$$

Where,

$a_7 = -2.567e-9$
$a_6 = -1.66e-6$
$a_5 = 0.3688$
$a_4 = 238.8$
$a_3 = 1.252e5$
$a_2 = 3.92e7$
$a_1 = 1.034e10$
$a_0 = 7.468e11$

$b_8 = 1.77e-12$
$b_7 = 4.045e-8$
$b_6 = 0.0002634$
$b_5 = 0.4327$
$b_4 = 316.5$
$b_3 = 1.408e5$
$b_2 = 4.529e7$
$b_1 = 1.138e10$
$b_0 = 7.985e11$

Figure 4.6 shows the implementation block diagram for phase current controllers.

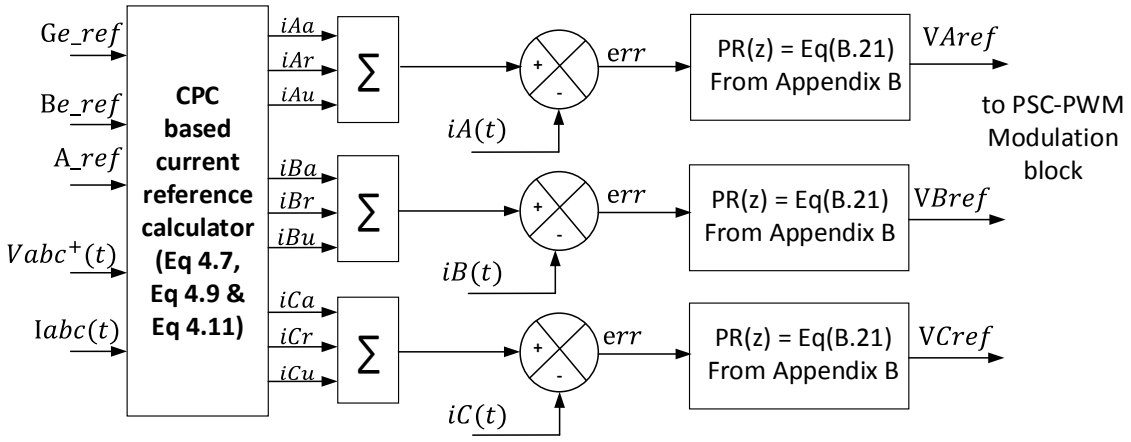

Figure 4.6 CPC based phase current control block diagram

4.2.2 Circulating Current Controller Design

The design of a circulating current controller using proportional resonant controller in the ABC frame is similar to phase current controller design with the slight differences in transfer function and resonant controller tuned frequency. Figure 4.7 shows the block diagram of circulating current control loop using PR controller. The resonant controller in this case is tuned to circulating current frequency which is 2nd harmonic of fundamental i.e. 120Hz

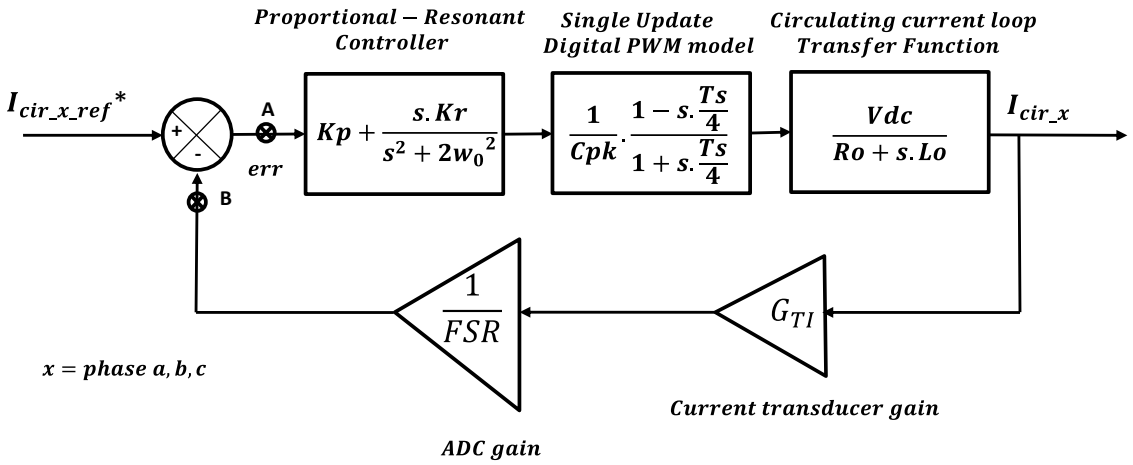

Figure 4.7 Circulating Current control loop block diagram

The design of controller gains is done by Naslin polynomial technique and the procedure is similar to phase current controller design and explained in Appendix B.2. From Appendix B.2 the closed transfer function of circulating current controller is obtained as,

$$G_{CL}(s) = \frac{a_7 s^7 + a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_8 s^8 + b_7 s^7 + b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \qquad (4.15)$$

Where,

$a_7 = -2.767e-9$ $\quad b_8 = 1.77e-12$
$a_6 = -2.153e-6$ $\quad b_7 = 4.02e-8$
$a_5 = 0.3951$ $\quad b_6 = 0.0002644$
$a_4 = 308.6$ $\quad b_5 = 0.4957$
$a_3 = 4.791e5$ $\quad b_4 = 612.5$
$a_2 = 1.988e8$ $\quad b_3 = 5.517e5$
$a_1 = 1.441e11$ $\quad b_2 = 2.872e8$
$a_0 = 1.288e13$ $\quad b_1 = 1.608e11$
$b_0 = 1.37e13$

Figure 4.8 shows the implementation block diagram of circulating current controllers.

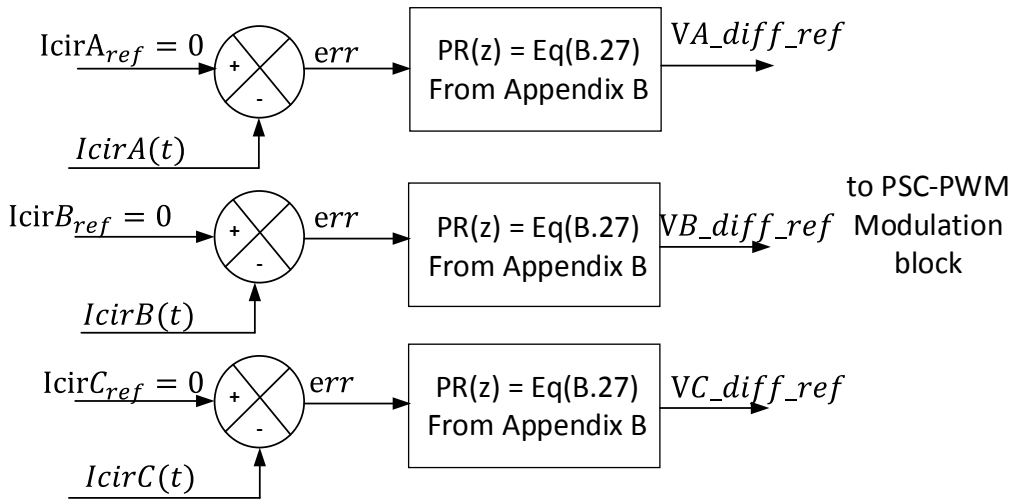

Figure 4.8 PR circulating current controller block diagram

4.2.3 Active and Reactive Power Controller Design

Active and reactive power controller design is similar as discussed in chapter 2 except that instead of computing instantaneous power using instantaneous grid voltage and phase currents the positive sequence voltage component of grid voltage and instantaneous phase currents are used to compute the instantaneous active and reactive powers. The formulae for computing active and reactive powers at the fundamental frequency with respect to positive sequence grid voltage components are given by equations (4.16) and (4.17).

$$P^{+}(t) = Va^{+}(t).Ia(t) + Vb^{+}(t).Ib(t) + Vc^{+}(t).Ic(t) \tag{4.16}$$

$$Q^{+}(t) = \frac{1}{\sqrt{3}}[(Vb^{+}(t) - Vc^{+}(t)).Ia(t) + (Vc^{+}(t) - Va^{+}(t)).Ib + (Va^{+}(t) - Vb^{+}(t)).Ic(t)] \tag{4.17}$$

Equations (4.16) and (4.17) consist of time domain positive sequence component of grid voltages. These components are not directly available. The information available

using RDFT based symmetric component decomposition is the positive sequence voltage magnitude and angles of each positive sequence phase voltage. Using this information instantaneous three-phase positive sequence voltage component present in the grid supply can be derived. Once the time-domain positive sequence voltage waveform is available then by using equations (4.16) and (4.17) active and reactive powers with respect to positive sequence voltage components can be found. Figure 4.9 shows the block diagram of this process.

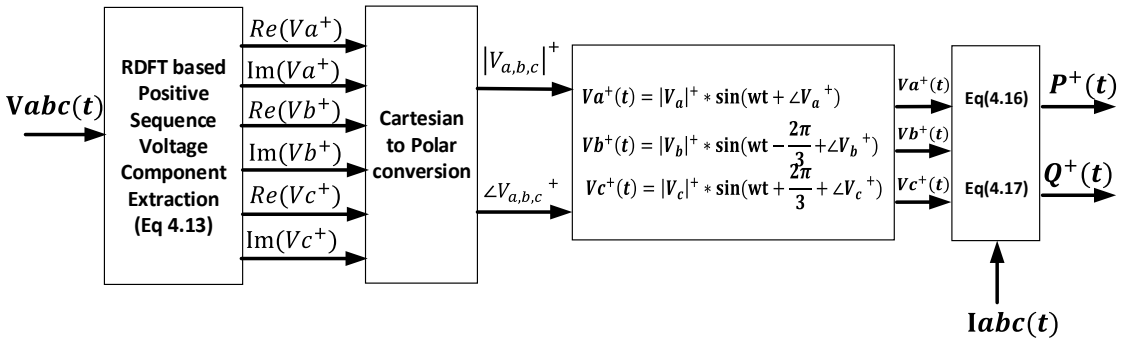

Figure 4.9 Block diagram of Instantaneous power computations

Figure 4.10 shows the interface between the power controllers and the phase current controllers. From Figure 4.9, once the active and reactive powers are available then they can be compared with the desired active and reactive power references. The active and reactive power controllers then produce required active and reactive current references respectively. The ratio of these required current references and magnitude of positive sequence voltage component gives the equivalent conductance and equivalent reactance references of the three phase system. The reference for unbalance admittance "A_ref" is set to zero to minimize any unbalance power that could result due to asymmetrical supply and/or unbalance load.

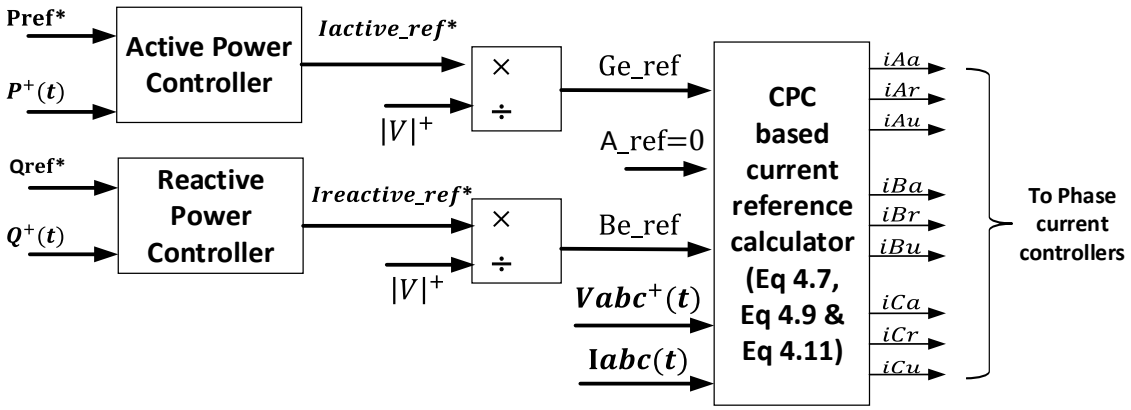

Figure 4.10 Block diagram of Power controllers interface with phase current controllers

Using equivalent conductance, reactance and unbalance admittance reference, instantaneous positive sequence grid voltage component and instantaneous phase currents the desired active, reactive and unbalance current component of each phase can be computed using equations (4.7) to (4.11). These desired reference currents are then available to phase current controller for further action.

4.3 SIMULATION RESULTS

This section discusses simulation results using CPC based control structure of Figure 4.4. Some new methods are also presented to improve the performance of MMC under balance as well as unbalance grid supply conditions.

4.3.1 CONTROLLER PERFORMANCE UNDER BALANCE CONDITIONS

Figure 4.11 shows the performance of CPC based control under balance supply conditions for Pac = 60KW & Qac = 0. Figure 4.11 (b) shows that the CPC controller produces sinusoidal phase currents during balance grid supply condition. Figure 4.11 (e)

shows active power and dc side power before and after circulating current controller is activated.

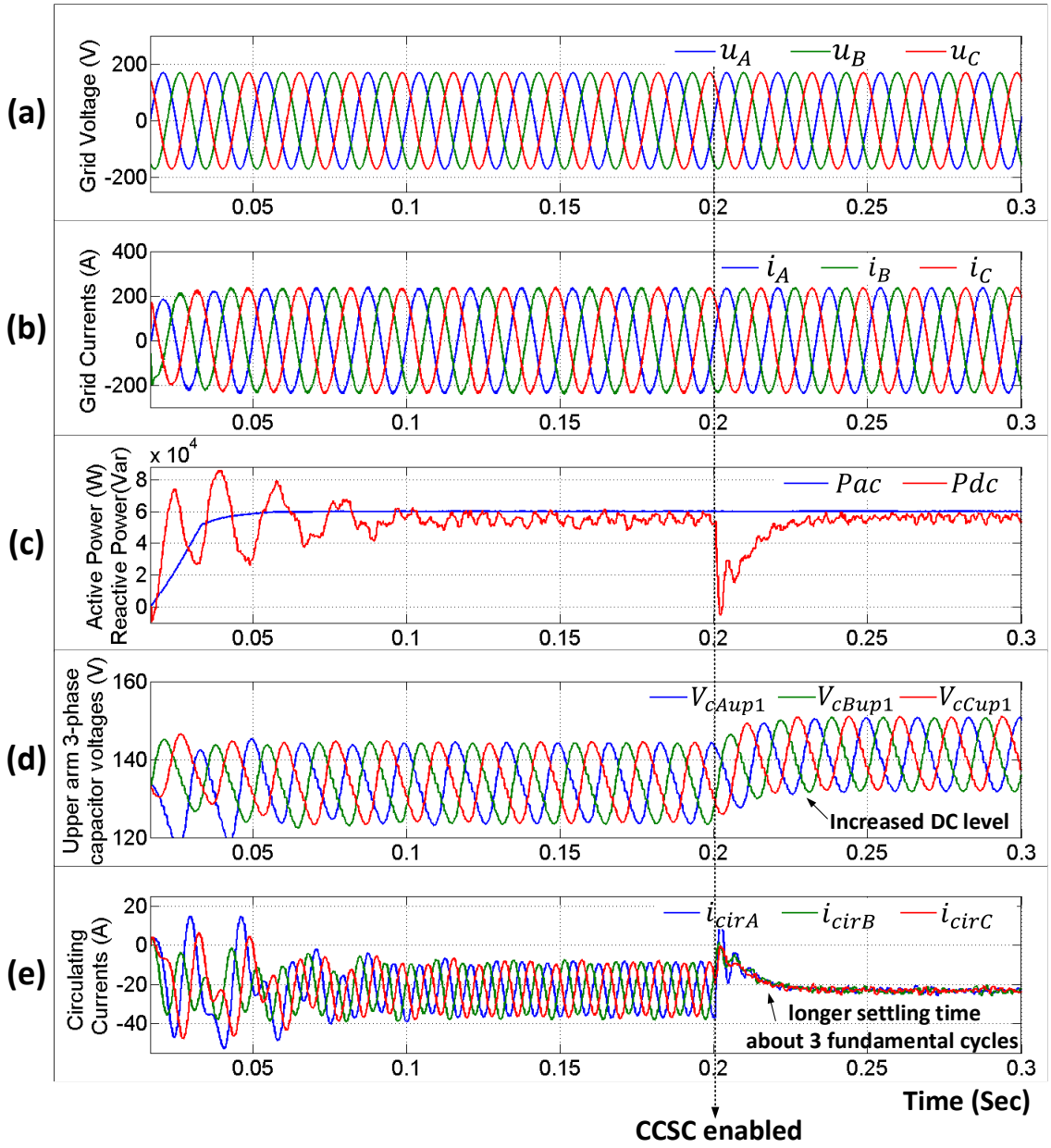

Figure 4.11 CPC based control performance under Balance supply condition

Figure 4.11 (d) shows that once the circulating current controller is activated it immediately minimizes the 2nd harmonic from the phase legs and -the only components left are dc current bias and switching harmonics. The dc current biases of each phase leg

add up to produce the dc bus current. The switching harmonics in three phase leg's current is not a symmetric three phase component and therefore they also add up and the addition is injected in dc bus current. It can be clearly observed from Figure 4.11 (e) that before CCSC is enabled the dc bus power or current (dc voltage is always constant due to an ideal DC source in the simulated system) has no switching harmonics but after CCSC is enabled it has switching harmonics. It is also observed that the CCSC has a settling time of about 0.1sec.

This large settling time could affect the performance of the CCSC during transients. Another important observation from Figure 4.11 (c) is that the DC level of sub-module capacitors changes after the CCSC is enabled. The reason behind the increase in DC level of capacitor voltages is certainly an undesired behavior and can severely affect the performance of MMC by limiting the available operating region during balance as well as unbalance supply conditions. Therefore, the effect of circulating current suppressing controller on capacitor voltages needs to be investigated and a solution to maintain the capacitor dc level needs to be found.

4.3.2 Effect of Circulating Current Control on Capacitor Voltages

The circulating current controller has two components i.e. DC bias and 2nd harmonic negative sequence component. The DC bias contributes to the DC bus current but the 2nd harmonic only circulates between three phase legs as long as it is a three-phase symmetric component. Any asymmetry in this three-phase 2nd harmonic component would result in ripples in DC bus current. In order to remove the 2nd harmonic from phase leg currents the CCSC controller injects dc bias and 2nd harmonic in the modulating

signal. The injected 2nd harmonic minimizes the circulating current. But the added dc bias in the modulating signal causes it to drift away from the 0.5 axis of symmetry. The modulating signal swings between 0 and 1. When the modulating signal of upper arm goes above 0.5 at the same time the modulating signal of lower arm goes below 0.5. This causes to create 180deg phase shifted voltages on upper and lower arm. The 0.5 axis of symmetry is important to keep the correct DC voltage level on all sub-module capacitors. When upper arm and lower arm modulating signals are symmetric about 0.5, it guarantees that at any given instant of time the total number of capacitors connected across the DC bus = N, where, 'N' is number of sub-modules in each arm.

It is desired that each capacitor must maintain their DC level all the time and the DC level across each capacitor is equal to (Vdc/N). This allows creation of a symmetric staircase waveform at the converter outputs (i.e. phase leg midpoints). However, if more than N numbers of capacitors are connected across DC bus then in steady state the voltage across each capacitor would be less than (Vdc/N) and if a lower number of capacitors are connected then in steady state the capacitor voltage would be more than (Vdc/N). Figure 4.12 illustrates the above explained phenomenon.

During balanced supply condition, before CCSC is enabled, the modulating signals (Figure 4.12 (a) and (b)) are symmetric about 0.5 which produces certain N_{ON} waveform. Addition of upper arm and lower arm N_{ON} is equal to 6 as shown in Figure 4.12 (e). This constant 6 number of capacitors across DC bus keeps all upper arm as well as lower arm capacitor dc level to a constant as given by,

$$\frac{Vdc}{N} = \frac{800}{6} = 133.33V$$

When the CCSC is activated at 0.2 second the modulating signal goes away from the 0.5 axis of symmetry. This means total number of capacitors connected across DC bus in each phase leg is not equal to N (or 6 in this case). In fact the total number of capacitors across DC bus lies somewhere between 6 and 4 and this causes to increase the steady state dc level across each capacitor. Figure 4.12 (f) shows that the capacitor voltage dc level is approximately 150Volts in steady state after the CCSC is enabled.

This behavior of the circulating current controller causes to put a limit on the amount of reduction that can be achieved in the circulating current 2nd harmonic without exceeding capacitor voltage ripple constraints. A trade-off between reduction in 2nd harmonic and capacitor voltage ripple would then be required to achieve the best possible result during balance and unbalance supply conditions.

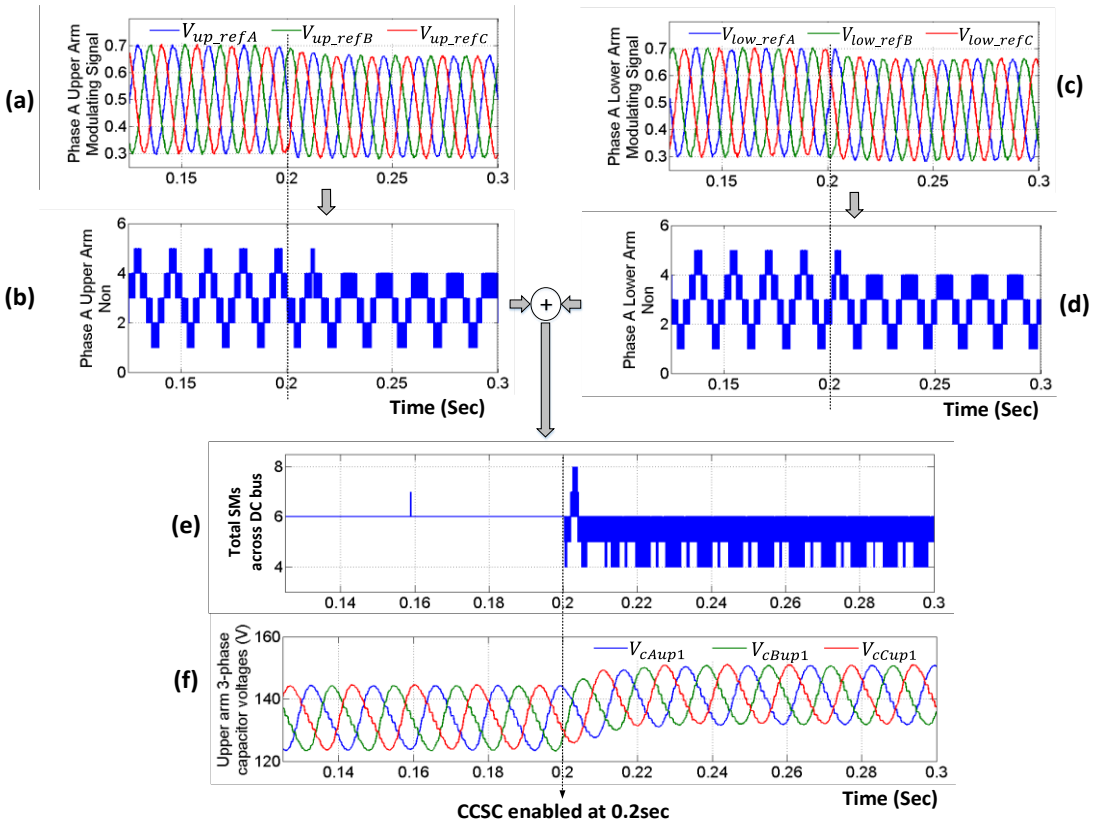

Figure 4.12 Effect of circulating control on modulating signals, N_{ON} and capacitor voltages

4.3.3 MODIFIED CIRCULATING CURRENT CONTROLLER

In order to overcome the limitation of traditional circulating current controller performance a technique is proposed that maintains the average value of the voltages across all sub-module capacitors during unbalanced current conditions. The block diagram of this modified CCSC technique is shown in Figure 4.13. In traditional circulating controller only upper and lower arm currents are added to compute circulating current. But this current also has dc component which affects the performance of circulating current controller by changing capacitor dc level. Therefore, a more accurate technique proposed in Figure 4.13. In this technique instead of subtracting one third of dc bus current from phase leg current the dc component of phase leg current can be extracted using RDFT algorithm and then subtract it from circulating current equation. This leaves behind only 2^{nd} harmonic component of circulating current. Due to this technique the circulating current controller only sees 2^{nd} harmonic components and only produces the control signal for minimizing it. The results are shown in Figure 4.14.

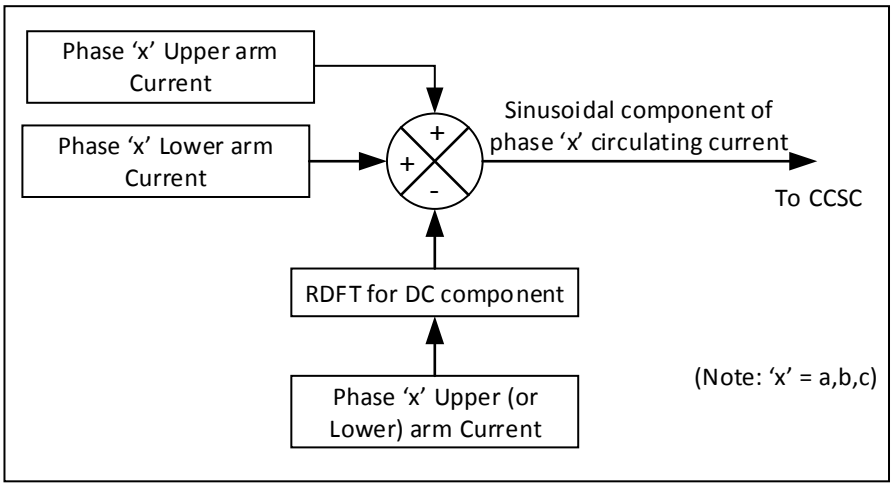

Figure 4.13 Block diagram of circulating current's 2nd harmonic extraction

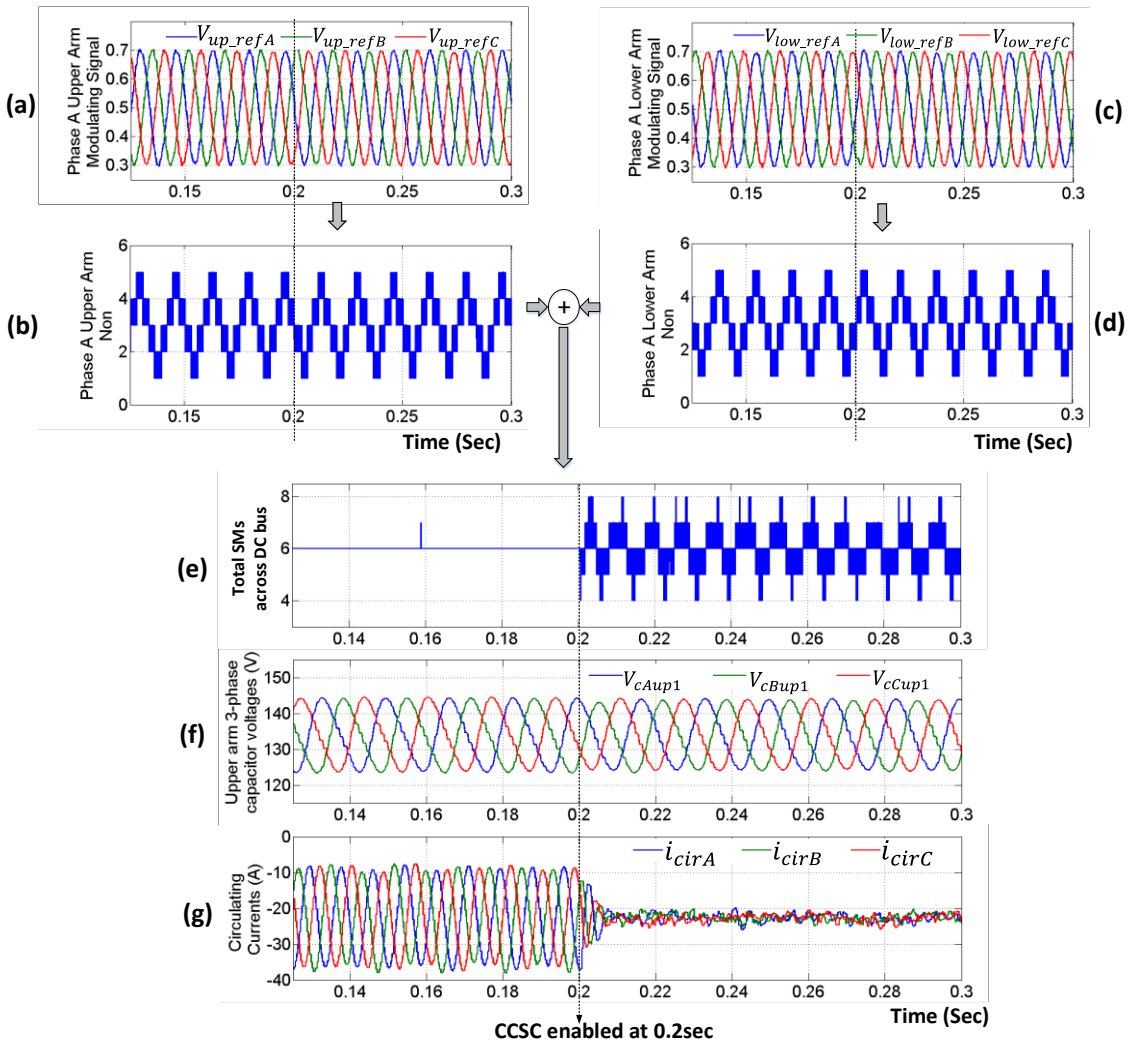

Figure 4.14 Modified Circulating current controller maintains capacitor's DC level

As shown in Figure 4.14 (a) and (b) during balance supply conditions before and after CCSC is enabled the modulating signal for upper arm as well as lower arm does not change its DC bias and it is fixed to 0.5; corresponding N_{ON} and their addition is shown in Figure 4.14 (b), (d) and (e). Figure 4.14 (e) shows that a 2nd harmonic control signal is added across phase leg total N_{ON}. It is clearly seen that 2nd harmonic is added on top of dc value of 6. That means in steady-state average value of capacitors across dc bus is maintained to 6 and the 2nd harmonic component is inserted to minimize the circulating current. Figure 4.14 (g) shows the circulating current minimizes to vary small value very

quickly and there is no transient either. Figure 4.14 (f) shows the capacitor voltages of 3 phase legs and it is pretty evident that their dc level is not at all affected by enabling of CCSC. These results show great promise to maintain the operating region of MMC with CCSC and improve it during unbalance supply compared to traditional control approaches.

4.3.4 CONTROLLER PERFORMANCE UNDER VARIOUS FAULT CONDITIONS

This section discusses performance of CPC based controller and modified CCSC for MMC during single-phase as well as two-phase grid fault conditions.

In order to study performance of CPC controller during unbalance situation it is required to define the technical meaning of voltage unbalance. According to [47] a definition of the percentage voltage unbalance can be given by using the ratio of negative sequence voltage component to the positive sequence voltage component. From [47] the percentage 'Voltage Unbalance' factor (% VU), or the true definition, is given by,

$$\%VU = \frac{negative\ sequence\ component}{positive\ sequence\ component} * 100 \tag{4.18}$$

The positive and negative sequence voltage components are obtained by resolving three-phase unbalanced line-to-ground voltages $V_a, V_b \& V_c$ into two symmetrical components $V_p \& V_n$. The two balanced components are given by,

$$Vp = \frac{Va + \alpha * Vb + \alpha^2 * Vc}{3} \tag{4.19}$$

$$Vn = \frac{Va + \alpha^2 * Vb + \alpha * Vc}{3} \tag{4.20}$$

Where, $\alpha = 1\angle 120^o$ and $\alpha^2 = 1\angle 240^o$.

Once the percentage voltage unbalance is known then the performance of proposed control system can be measured with respect to percentage unbalance.

By using RDFT modules the grid voltage can be decomposed into fundamental positive and negative sequence components. The percentage unbalance can be then found using equation (4.18).

Figure 4.15 shows performance of the proposed controller under moderate and severe unbalance conditions in the MMC system. The term VU at the top of figure is used as an abbreviation for 'Voltage Unbalance'. As shown in Figure 4.15 (a) initially a single phase to ground fault occurs at 0.2 sec which give approximately 50% unbalance and two-phase to ground fault occurs at 0.4 sec creating almost 100% unbalance. Figure 4.15 (b) shows the resulting phase currents whereas Figure 4.15 (e) shows active power and dc side power. As can be seen from the active power waveform, the CPC controller maintains the active power reference command during balance as well as severe unbalance conditions. After the fault transient, the active power returns to the desired reference value. Also, no current and power oscillations are observed in these waveforms. The phase currents during unbalance are also sinusoidal and symmetric (magnitude as well as phase).

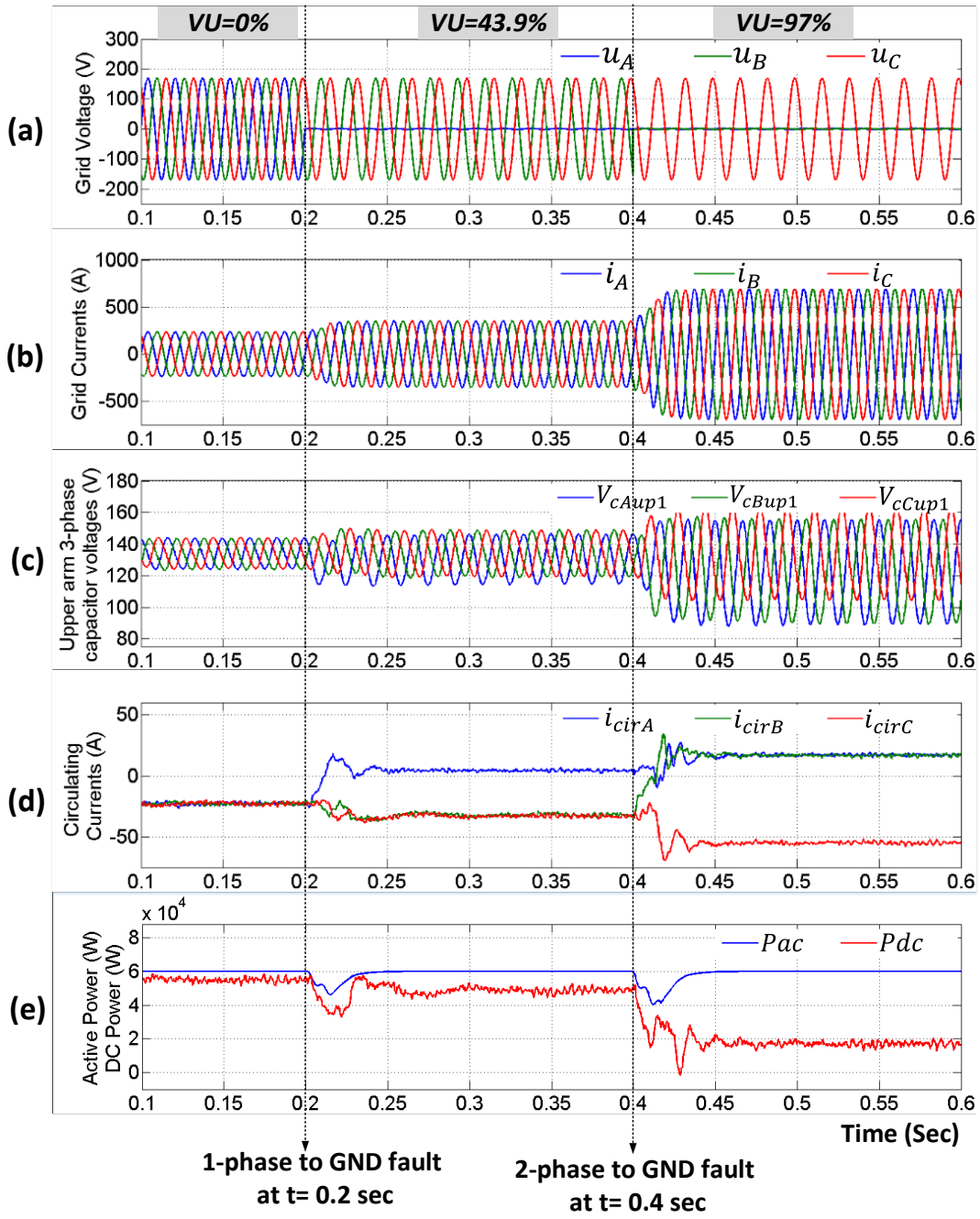

Figure 4.15 CPC based control performance under 1-phase to GND fault

The penalty for keeping the active power constant during unbalance conditions is that the peak value of phase currents is increased in order to compensate for the reduction in RMS value of three-phase voltage. During two-phase to ground fault only one phase has source of energy and therefore large currents needs to be drawn from that phase and

distribute energy to the other two phases to maintain desired active power level, symmetric currents and also to keep the sub-module capacitors (especially the phases under fault) charged to desired level all the time.

Due to the increased RMS value of phase currents the I^2R losses in the arm inductors and semiconductor devices also increases which causes to decrease the DC power level. Note that AC power is same as before the fault but the converter internal losses increases, therefore, less power is transferred to the DC side during unbalance conditions. From Figure 4.15 (d) shows the circulating currents which are also stable but changes as unbalance occurs. Figure 4.15 (c) shows the upper arm sub-module capacitor voltages of three-phase legs (one capacitor from each) and it is clearly seen that as RMS value of phase current increases the fundamental ripple of capacitor voltage also increases which could go well beyond (+/-) 10% of nominal value.

In Figure 4.15 (e) it can be seen that although the active power is maintained during unbalance the dc side power is significantly lower. One possible strategy to maintain dc side power constant during unbalance is discussed in following section.

4.3.4.1 MAINTAINING DC POWER CONSTANT DURING UNBALANCE CONDITIONS

In order to keep dc side power constant a simple method is proposed. The instantaneous dc side power is compared with desired dc power and the remainder is added to the active power reference. This method can be accomplished by making some simple modifications in the existing control structure. The equation used for this method is as shown below.

$$P_{ac_{ref_{new}}}(t) = P_{ac_{ref_{original}}} + (P_{dc_{desired}} - P_{dc}(t)) \quad (4.21)$$

The implementation block diagram for this equation is shown in Figure 4.16.

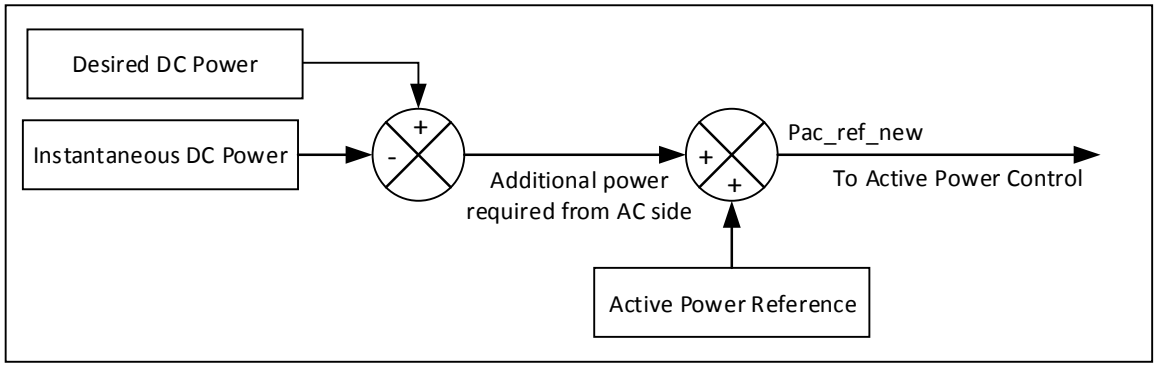

Figure 4.16 Method for keeping DC side power constant

Figure 4.17 shows the result of proposed strategy during unbalance condition. From Figure 4.17 (e) it is evident that during single phase fault the active power is increased in order to compensate for the losses caused by converter ckt and hence the dc power is closer to the desired reference value compare to Figure 4.17 (e).

As the voltage unbalance is further increases during two-phase to ground fault the active power reference is increased to much higher value but in this time the I^2R losses are so high that only negligible power is sent to dc side. Therefore, this method fails to achieve desired goal during severe unbalance conditions.

From Figure 4.17 a conclusion can be made that although this CPC based control structure maintains desired active power reference, sinusoidal & symmetric currents during unbalance it is not suitable in practical systems due to the large value of phase currents, capacitor voltage ripples and power losses during unbalance conditions.

Therefore, in order to ensure that the control maintains within a feasible operating region some modifications are needed as discussed in the following section.

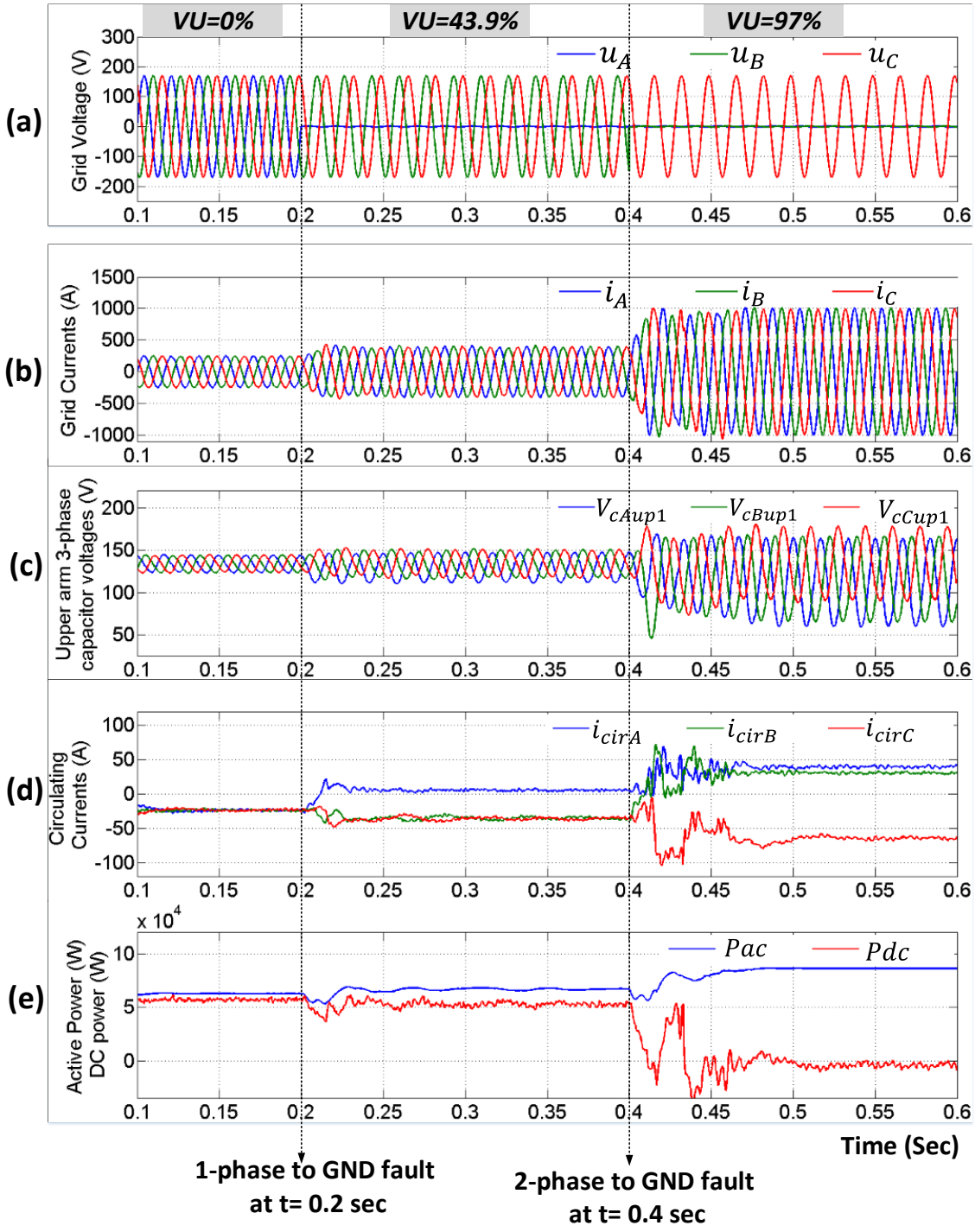

Figure 4.17 Keeping DC power constant irrespective of fault

4.3.4.2 LIMITING PEAK PHASE CURRENTS UNDER GIVEN CONSTRAINT

As explained in the previous section the requirement for keeping active power constant during unbalance is that the phase current peak value must be increased. In practical applications the increase in peak values of currents could easily exceed the maximum tolerable current limits of semiconductor as well as passive devices. Therefore, to avoid exceeding the device current constraints some technique must be implemented to avoid device overcurrent during fault conditions. This section proposes a simple method to achieve this goal.

In this method the active and reactive power references are defined as a function of instantaneous normalized three-phase RMS value of positive sequence fundamental voltage component. During balance supply this coefficient is equal to 1 and the active and reactive power references are unchanged. But during unbalance this coefficient would decrease (min possible value is 0) and hence the active and reactive power references would also reduce proportionally. Since power references are reduced in proportion to the reduction in three-phase RMS value of grid voltages the phase current magnitude should remain constant.

An equation that defines the relationship between modified AC power reference and grid voltages is as shown below,

$$P_{ac\_ref\_new} = P_{ac\_ref\_original} * k \tag{4.22}$$

Where,

$$k = \frac{(V_{A_{rms}} + V_{B_{rms}} + V_{C\_rms})}{3 * V_{ph-gnd}} \tag{4.23}$$

During balanced supply conditions k=1, but during fault conditions k would decrease depending on the magnitude of fault. Figure 4.18 shows the block diagram of this method. The symbol 'x' represents multiplication.

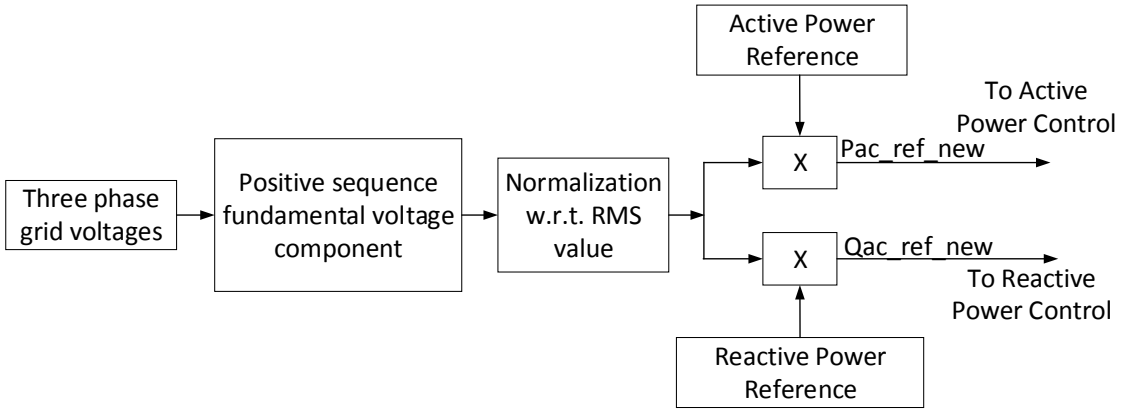

Figure 4.18 Method to maintain phase current within constraints

Figure 4.19 shows the effectiveness of the proposed method to keep phase currents constant during unbalance conditions. The superiority of this method along with CPC control over traditional methods is highly evident looking at Figure 4.19 (b) and (e) i.e. phase currents and active/dc powers. Although the fault event is step change the power references changes ever so smoothly that the phase currents do not at all show any transient behavior during or after severe fault events.

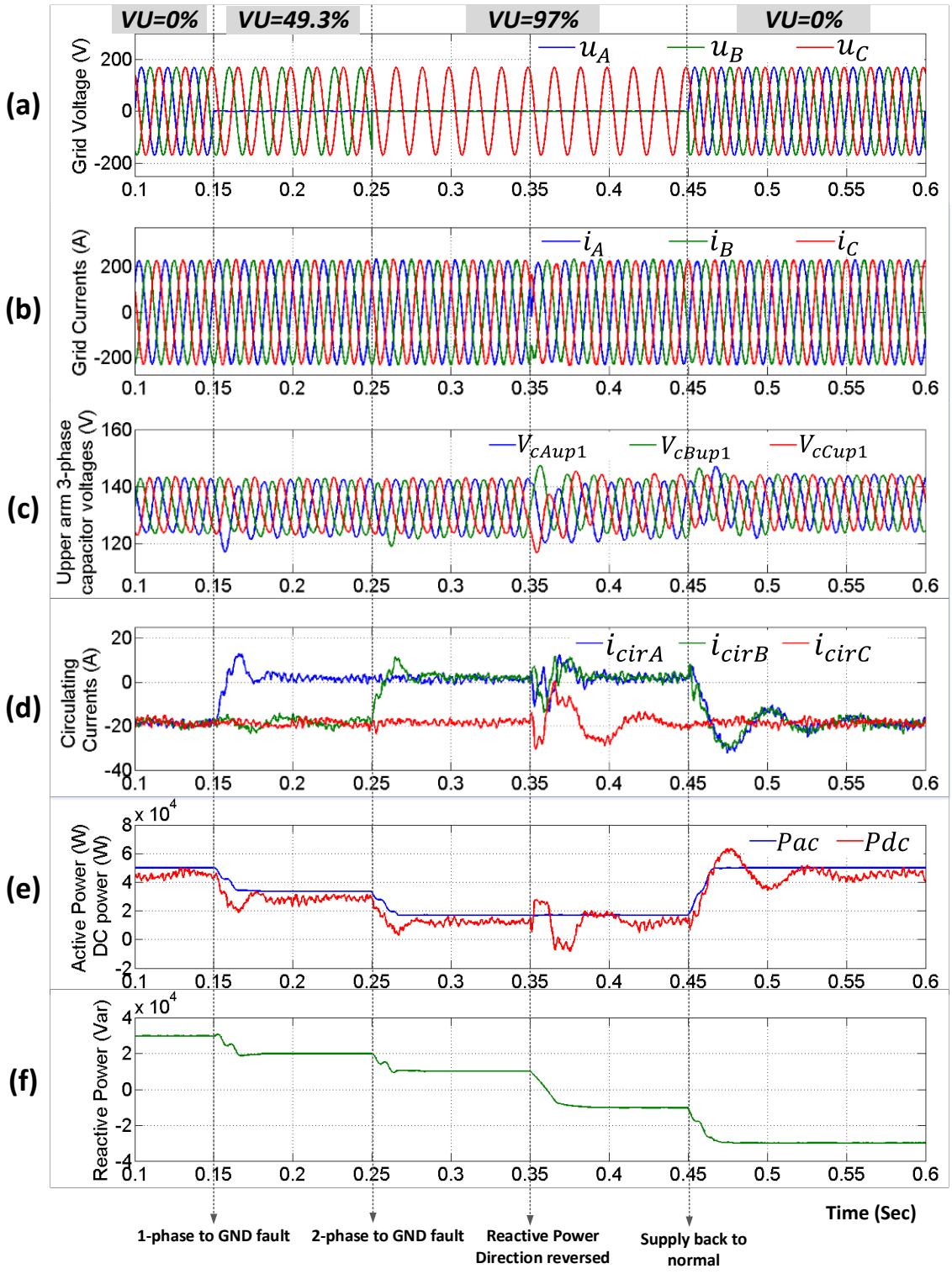

Figure 4.19 Keeping phase currents constant irrespective of fault

4.3.4.3 PERFORMANCE EVALUATION UNDER PHASE TO PHASE FAULT

The performance is next evaluated for phase-phase faults. The phase-phase fault is generated by injecting unbalance impedance between grid supply and the MMC system. The unbalance impedance causes to change voltage magnitudes as well as their phase relationship. The block diagram for creating phase-phase faults is shown in Figure 4.20.

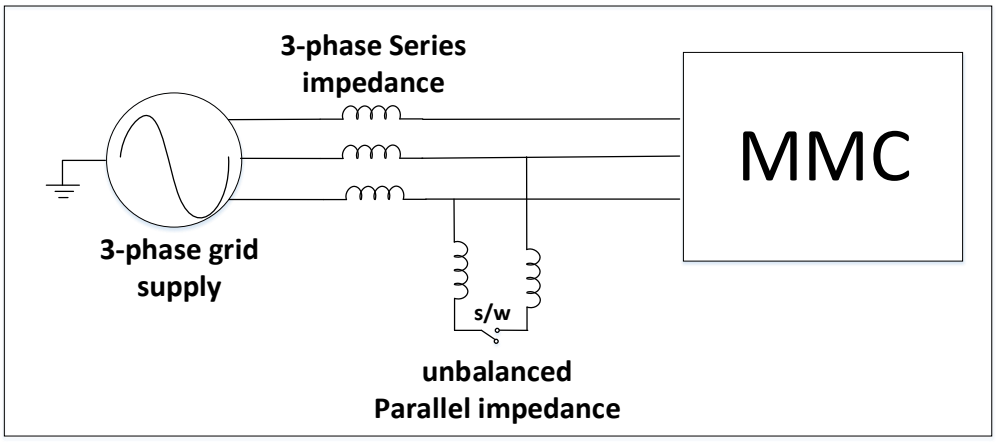

Figure 4.20 Phase to phase fault creation method

By using the circuit shown in Figure 4.20, a phase-to-phase fault that generates approximately 50% unbalance was simulated and the resulting waveforms are shown in Figure 4.21. From the results it can be seen that the phase currents are symmetric all the time (even during transients). Capacitor voltages return to steady-state after about 3 fundamental cycles. Circulating currents and their dependent dc current have slight transients but they also reach steady state within 0.2 sec. It is important to note that any transient on dc side would take slightly longer to reach steady state than ac side because the large value of sub-module capacitances introduces longer time constants for energy routing through the system.

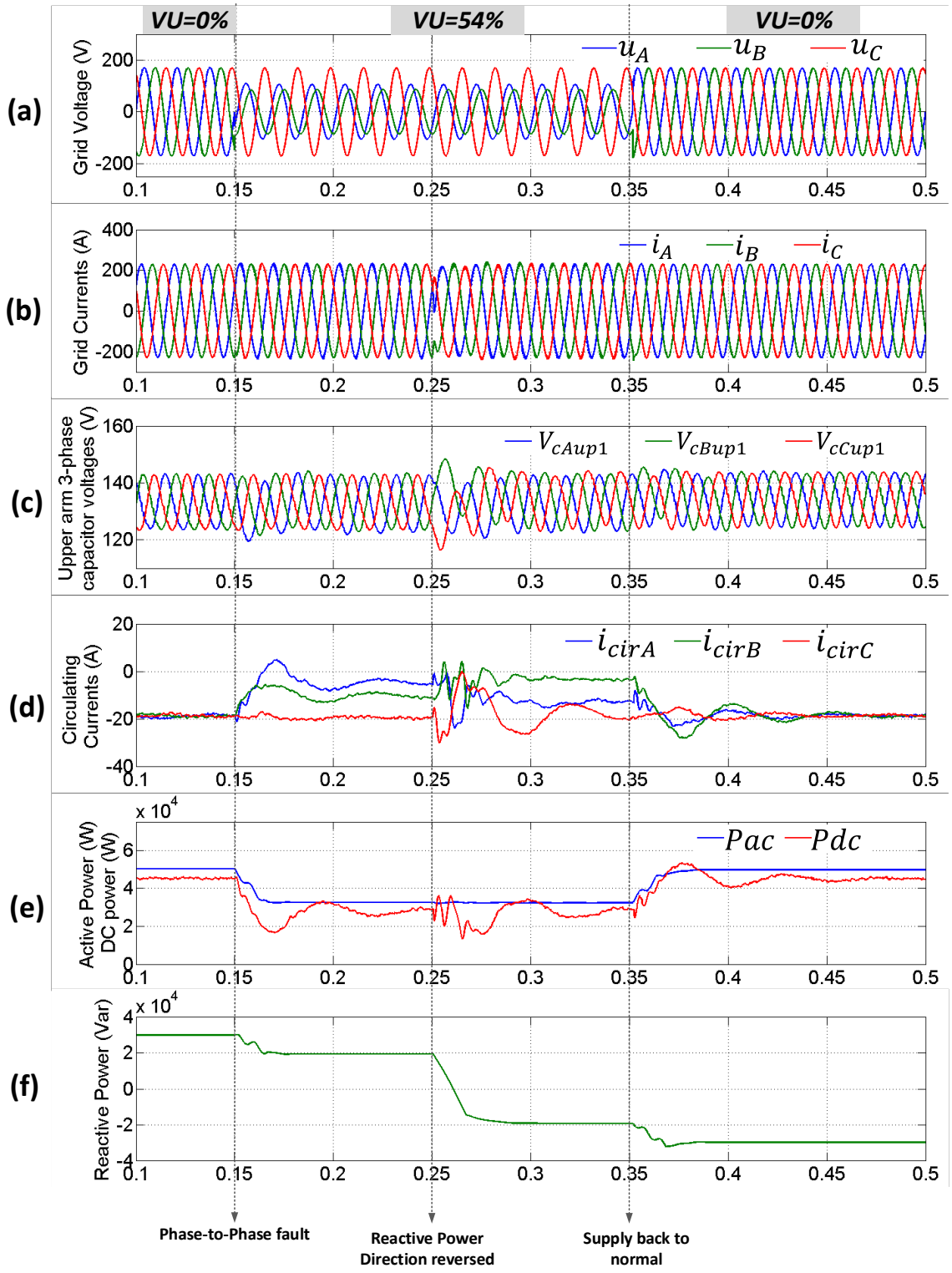

Figure 4.21 Performance under phase-to-phase fault

4.3.4.4 PERFORMANCE EVALUATION UNDER NON-SINUSOIDAL SUPPLY VOLTAGES

Previous sections discussed different fault conditions but the supply only had fundamental voltage component. This is not always the case in practical systems. Due to various types of non-linear loads distributed in power systems the supply voltage at the point of connection to a MMC may have some level of distortion.

Here the control will be further extended in order to prevent performance degradation due to supply voltage distortion The modification is done by adding RDFT module to extract the fundamental component from grid supply voltages. The RDFT module is computationally efficient and can be used for extracting the desired frequency components as explained earlier in this chapter. Although individual RDFT block only extracts one frequency component, by using combination of RDFT modules can allow to extract positive, negative and zero sequence components of that desired frequency component. This further increases the efficiency of RDFT modules when implemented on DSP processor. Figure 4.22 shows the method to real-time extraction of fundamental frequency component as well as positive and negative sequence components present in the grid supply.

The simulation model is modified to incorporate the method described in Figure 4.22. The CPC controller now acts only on positive sequence voltage component to produce sinusoidal phase currents and desired power output. This new control structure is also validated for non-sinusoidal supply conditions and the results are shown in Figure 4.23.

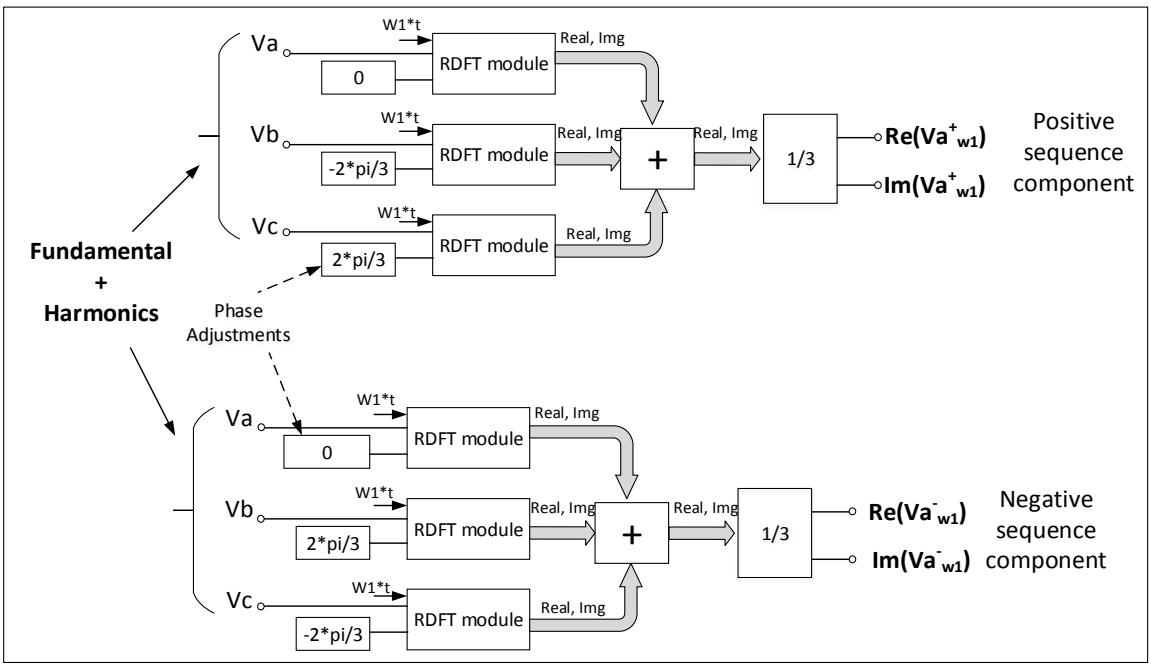

Figure 4.22 RDFT based fundamental frequency and symmetric component extraction

As shown in Figure 4.23 several different harmonics are injected in grid voltages at 0.2 sec. The injected harmonics are 2nd, 3rd, 4th, 5th, 6th, and 7th with 10Vrms each and selected random phase angles. This produces grid voltage THD of about 25% as shown in Figure 4.23 (C).

The resulting phase current THD is approximately 2.5%. The active and dc powers have negligible effect of harmonics injected in grid voltage. As shown in Figure 4.23 (b) & (d) the phase current's symmetry and sinusoidal shape are barely affected by non-sinusoidal grid voltages with high THD of about 25%. DC side power is also only slightly affected.

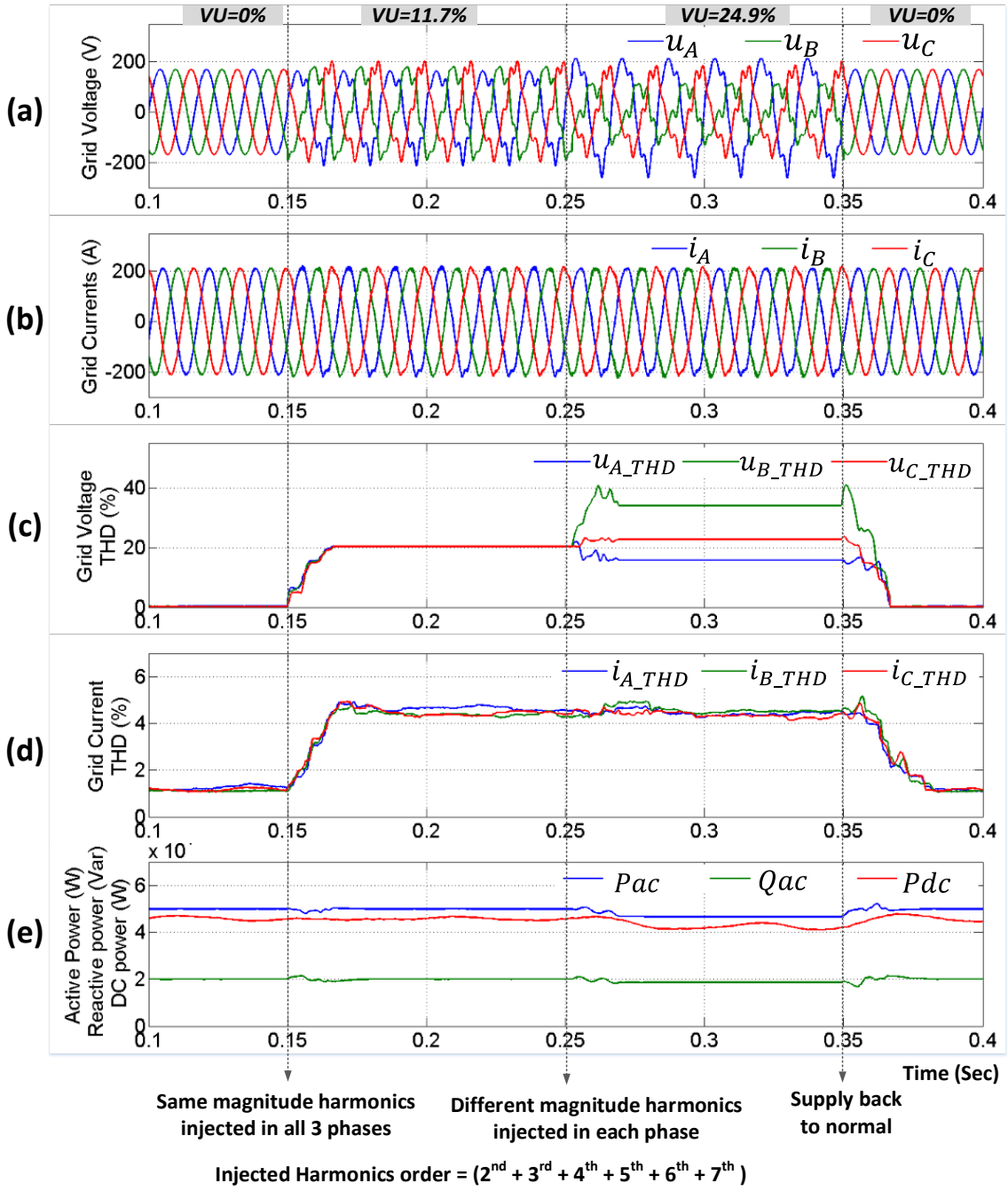

Figure 4.23 Performance under non-sinusoidal supply conditions

This chapter discussed some novel methods (CPC based control for MMC, modified CCSC, modified power reference generation etc.) to improve the performance of modular multilevel converter during unbalance supply conditions that includes phase

to ground faults, phase to phase faults and non-sinusoidal supply voltages. The CPC based control assures that only positive sequence symmetric currents are always injected in to the grid. One of the main concerns in MMC during unbalance supply conditions is to keep the capacitor voltages balanced at their nominal DC voltage value. The modified CCSC method accomplishes this goal. Together these methods produce ripple free power on both ac and dc sides of a MMC. The modified power reference generation method assures that the current limits of semiconductor devices do not exceed their maximum limit by adjusting power reference as a function of three-phase RMS voltage value.

CHAPTER 5

ESTIMATION AND EXTENSION OF MODULAR MULTILEVEL CONVERTER OPERATING REGION UNDER UNBALANCE SUPPLY

Modular Multilevel Converters are highly dynamic, nonlinear and time varying systems. CPC based control system that was developed in chapter 4 assures good performance of a MMC under balance as well as any type of unbalanced supply voltages. It is important to know the operating region of the MMC as a function of all expected supply conditions in order to optimize parameters of the MMC system during the design process. The function of the operating region with respect to key system parameters also ensures that the operating region can be maximized.

This dissertation proposes a novel approach for determining the operating region of a MMC under various input conditions using a simple average model that allows quick calculation of many system parameters by solving a few equations as will be explained in the following section.

The goal of this method is to derive a set of equations that solve for submodule capacitor voltages (fundamental and 2^{nd} harmonic) and circulating current amplitude for given grid voltages and power references. Since the average model equations can be solved very quickly results can be obtained for many input conditions within a reasonable time by computer. Results presented here were obtained using Matlab.

5.1 DEVELOPING AVERAGE MODEL FOR ESTIMATION OF VARIOUS MMC PARAMETERS

Consider a simplified one phase leg of MMC system as shown in Figure 5.1.

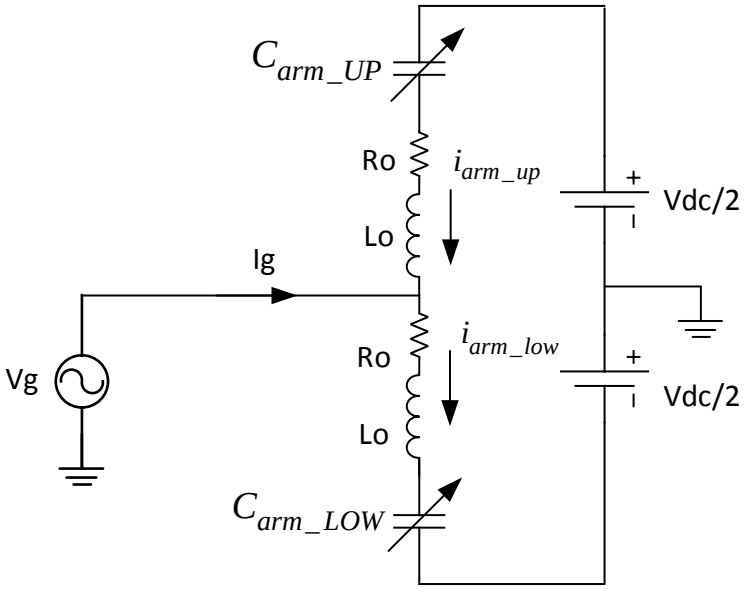

Figure 5.1 MMC phase leg with average model of arm capacitance

In this the arm sub-modules are represented as equivalent single linearly variable capacitor whose capacitance is inversely proportional to arm reference signal and its voltage is directly proportional to arm reference signal. The assumption of single linearly variable capacitor is done by neglecting switching harmonics present on the capacitor voltages and assuming that all the capacitors in an arm has exactly same voltage waveform. This assumption loses the information about capacitor voltage unbalance and effect of switching frequency but it does preserve the information about average value of capacitor voltage, fundamental voltage ripple magnitude on capacitors.

Using CPC theory fundamentals to the three-phase average model MMC system the following equations can be written,

$$P = \frac{{V_g}^2}{R} = {V_g}^2 * G_e; \quad Q = \frac{{V_g}^2}{X} = {V_g}^2 * B_e \tag{5.1}$$

where, P is Active power, Q is reactive power, V_g is grid voltage, G_e and B_e are equivalent conductance and reactance seen from grid side, respectively.

The CPC control method that is proposed in chapter 4 considers fundamental positive sequence grid voltage component as a reference voltage component. Therefore, the equation for active and reactive grid current components can be written as,

$$\begin{aligned} I_{active} &= {V_g}^+ * G_e \\ I_{reactive} &= {V_g}^+ * B_e \end{aligned} \tag{5.2}$$

Total grid phase current then becomes,

$$I_g = I_{active} + I_{reactive} \tag{5.3}$$

Using KVL the phase current can be written as,

$$I_g = \frac{V_g - V_{conv}}{Ro + jXLo} \tag{5.4}$$

where, V_{conv} is the virtual converter voltage created by combination of upper and lower arm inserted voltages. The equation for V_{conv} is given by,

$$V_{conv} = \frac{Vc_{arm_{LOW}} - Vc_{arm\_UP}}{2} \tag{5.5}$$

The converter voltage V_{conv} is direct function of upper arm and lower arm inserted voltages whereas the upper and lower arm voltages are direct function of their respective modulating (also called Vref) signals. Therefore, V_{conv} is also direct function of Vref.

From the control structure of MMC the Vref can be solved as a function of V_{conv}.

$$V_{ref} = \frac{V_{conv} + \frac{V_{dc}}{2}}{V_{dc}} \tag{5.6}$$

Above formulae allows to directly calculate control Vrefs by simply using active/reactive power reference and instantaneous grid voltages. By knowing the Vrefs the sub-module capacitor voltage ripple and circulating current magnitudes can be computed.

The factors that decide the voltage waveform of capacitor are Vref, arm current, number of sub-modules in the arm and the voltage balancing algorithm. As explained in chapter 2, the sub-module capacitors are inserted and removed to/from the arm as defined by Vref (sinusoidal wave shape). Due to this fact the total capacitance inserted across the arm is also function of Vref The capacitance inserted across the arm, also called C_{arm}, must be known in order to find out voltage ripple shape of sub-module capacitor. The arm current of MMC flows through this C_{arm} which induces voltage ripple across all the sub-modules in the arm. This ripple actually consists of many harmonics (which will be shown later in this section), but the fundamental and 2nd harmonics are most important and dominant ones. The fundamental frequency ripple is direct function of active and reactive power, whereas, the 2nd harmonic voltage (and other negligible higher order even harmonics) is the result of varying capacitance across the arm and causes circulating current to flow within the phase legs. The arm capacitance is series connection of sub-module capacitors. The arm capacitance can be given by the equation,

$$C_{arm} = \frac{Co}{N_{ON}} \tag{5.7}$$

where, N_{ON} is number of sub-modules to be connected in the arm and Co is sub-module capacitance.

In practice, C_{arm} & N_{ON} are discrete staircase waveforms which are functions of Vref, but for average model those quantities can be assumed to be a linear function of Vref. This greatly simplifies relationship between Vrefs, arm capacitance and arm inserted voltages.

A linear version of N_{ON} can be written as,

$$N_{on} = V_{ref} * N \tag{5.8}$$

where, 'N' is total number of sub-modules in an arm.

The C_{arm} then becomes,

$$C_{arm} = \frac{C_o}{V_{ref} * N} \tag{5.9}$$

The arm current is given by,

$$I_{arm} = \frac{I_g}{2} \tag{5.10}$$

Note that both upper and lower arm currents have same magnitude but they are180 deg. phase shifted.

By knowing C_{arm} and I_{arm} the total voltage change across the arm capacitor over one fundamental period can be found. Note that, I_{arm} is sinusoidal, but C_{arm} is inversely proportional to sinusoidal term Vref. The solution for current flowing through arm capacitor is given by following equation,

$$I_c = I_{arm} = \frac{d}{dt}(Vc_{arm}) \tag{5.11}$$

Solving for Vc_{arm},

$$\Delta Vc_{arm}(t) = \frac{1}{C_{arm}(t)} * \int_0^{2\pi} I_{arm}(t) * dt \tag{5.12}$$

Solution of above equation gives total voltage ripple across the arm capacitor over one grid fundamental cycle. This total voltage ripple is distributed equally across each sub-module capacitor of that arm due to the use of voltage balancing algorithm. This algorithm sorts and selects capacitors to be inserted whenever there is change in N_{ON}. Due to this action, any voltage ripple that appears across the arm is equally distributed across all the sub-module capacitors in that arm.

Therefore, the voltage ripple across each sub-module can be given by,

$$Vc_x = \frac{\Delta Vc_{arm}}{N} \tag{5.13}$$

where, 'N' is total number of sub-modules in an arm, and 'x' is sub-module number from 1 to N

Once the voltage ripple waveform over one fundamental cycle is known then the harmonic contents in that ripple can be computed. Chapter 4 discussed that RDFT provides a very simple and fast computing solution for extracting frequency components in time-domain. This RDFT technique can be used to extract 1st and 2nd harmonic components in this capacitor voltage ripple (only need to solve over one fundamental cycle). Note that the 2nd harmonic of capacitor voltage ripple has same magnitude and

phase for both upper and lower arms. That means they both add up in the phase leg. This phenomenon can be represented by an equivalent circuit of Figure 5.2.

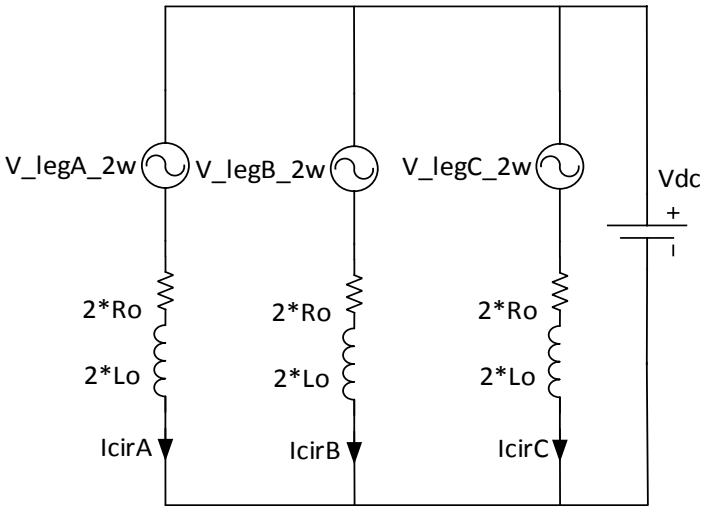

Figure 5.2 Equivalent circuit of circulating current model

From Figure 5.2 it is shown that the equivalent 2nd order harmonic voltage source in series with phase leg inductors will result in a 2nd order harmonic current that flows within the three phase legs of MMC. The magnitude of this current can be obtained by using following equation,

$$I_{cir\_2w} = \frac{V_{Leg\_2w}}{(2R_o + jw2L_o)} \tag{5.14}$$

Using equations (5.1) to (5.14) the capacitor voltage ripple and circulating current magnitudes can be easily found as a function of grid voltage and active/reactive power references. Equations (5.9), (5.12) and (5.13) are needed to be solved in time domain over one fundamental cycle while all other equations can be solved in frequency domain. It is necessary to do the time domain calculations since those equations have division by sinusoidal and integration terms. Solving above equations in Matlab results were obtained for various grid voltage and power reference combinations. The results are compared

with simulation model results in order to validate the accuracy of proposed method. The results are shown in Figure 5.3 to Figure 5.5.

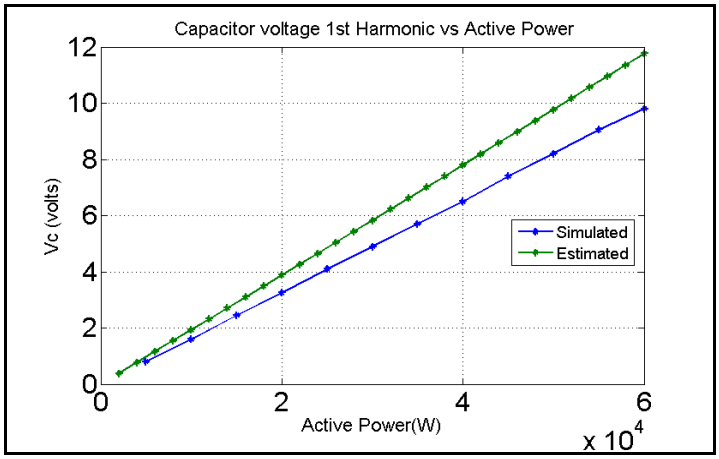

Figure 5.3 Simulation and Average model comparison for Vcw_1_pk vs Active power

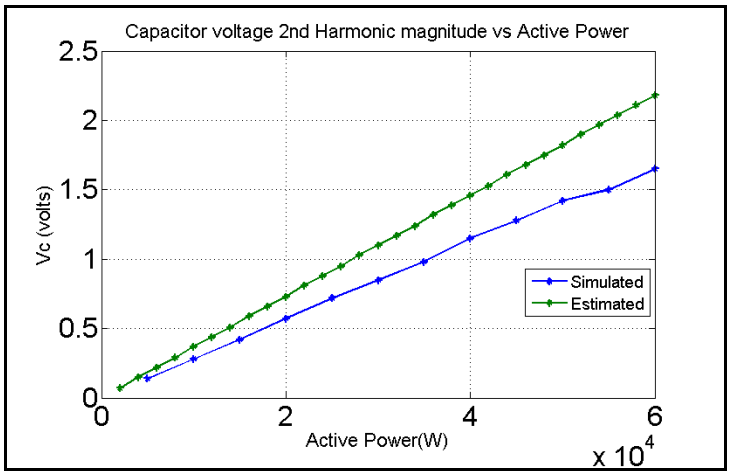

Figure 5.4 Simulation and Average model comparison for Vcw_2_pk vs Active power

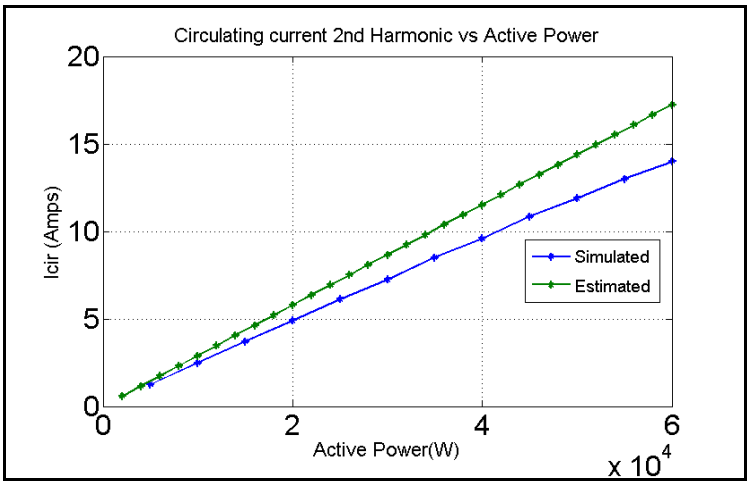

Figure 5.5 Simulation and Average model comparison for Icir_pk vs Active power

Figure 5.3 to Figure 5.5 gives a good estimate of desired MMC parameters as a function of active power but one drawback is that as active power increases the difference between estimated value and simulated value also increases. This is due to the fact that the estimation is based on average value model of MMC where the arm capacitance, upper arm and lower arm inserted voltages are linear function of time. Whereas, in simulation these parameters are affected by simulation time step, switching frequency, controller performance and also are discrete function of time.

Due to these reasons there is a fundamental difference between theoretically estimated value and simulated value. This difference can be defined as a percentage error and the percent error should be constant over the entire range of operation. If this percentage error can be corrected in the average model then the values estimated by average model should closely match with the values obtained by simulation. As an example, the percent error is found by comparing the values for 10kW. At 10kW Vc_sim=1.32V and Vc_estimate=1.6V. Since the error if found with respect to simulated results the equation for finding error is given by,

$$\%Error = \left(\frac{(Vc_{sim} - Vc_{estimate})}{Vc_{sim}} \right) * 100$$

This equation gives error of 23%. This error gives correcting factor of Kerr = (1-0.23) = 0.77. This factor is then included in the average model and then new results are computed for the similar input conditions as before and the comparison results are shown in Figure 5.6 to Figure 5.8.

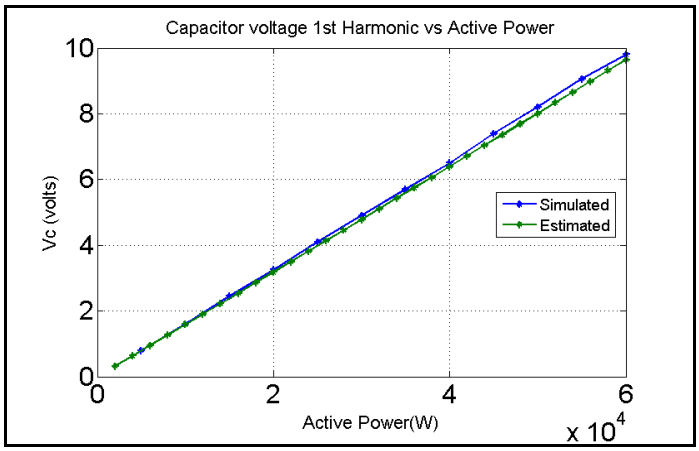

Figure 5.6 Simulation and Average model comparison for Capacitor voltage peak fundamental ripple vs Active power (with error compensation)

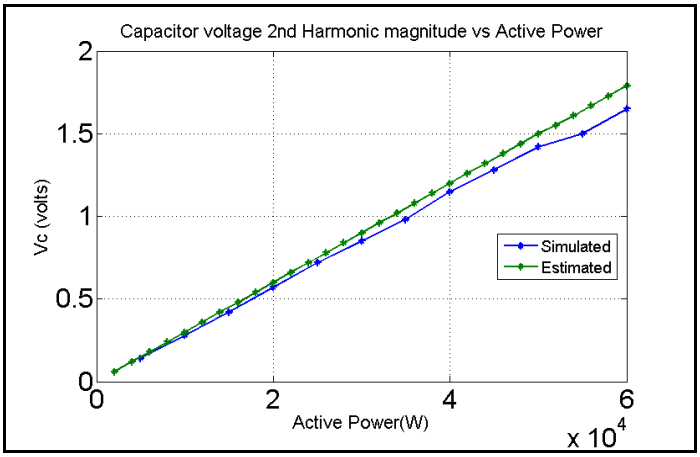

Figure 5.7 Simulation and Average model comparison for Capacitor voltage peak 2nd harmonic ripple vs Active power (with error compensation)

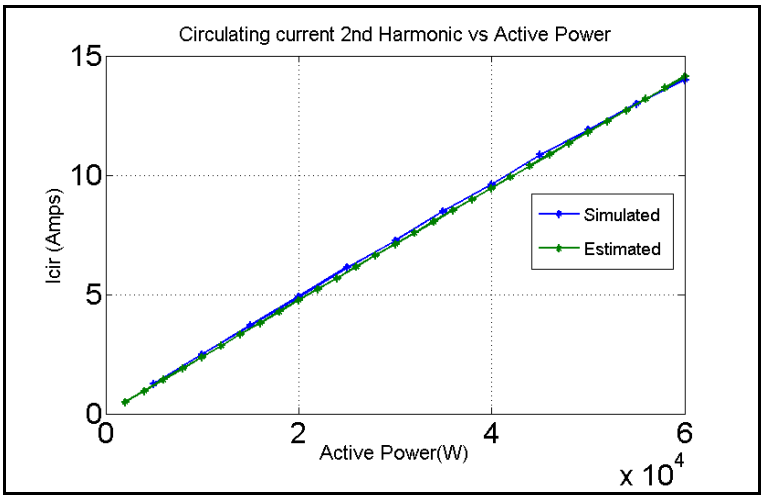

Figure 5.8 Simulation and Average model comparison for circulating current peak vs Active power (with error compensation)

Figure 5.6, Figure 5.7 and Figure 5.8 show that after adjusting for the error factor a very close match between simulated values and estimated values was obtained using average model of MMC. Upon validating the estimation method the operating region of some system parameters can be easily obtained as a function of various combinations of supply voltages and power references. A big advantage of this method is that it takes very short time to obtain the results as compared to simulation method.

Using the above method the variation of sub-module capacitor peak voltage as a function of active and reactive powers is computed under balance supply and results are shown in Figure 5.9. Similarly, the variation of peak circulating current as a function of active and reactive powers is also computed under balance supply and the results are shown in Figure 5.10.

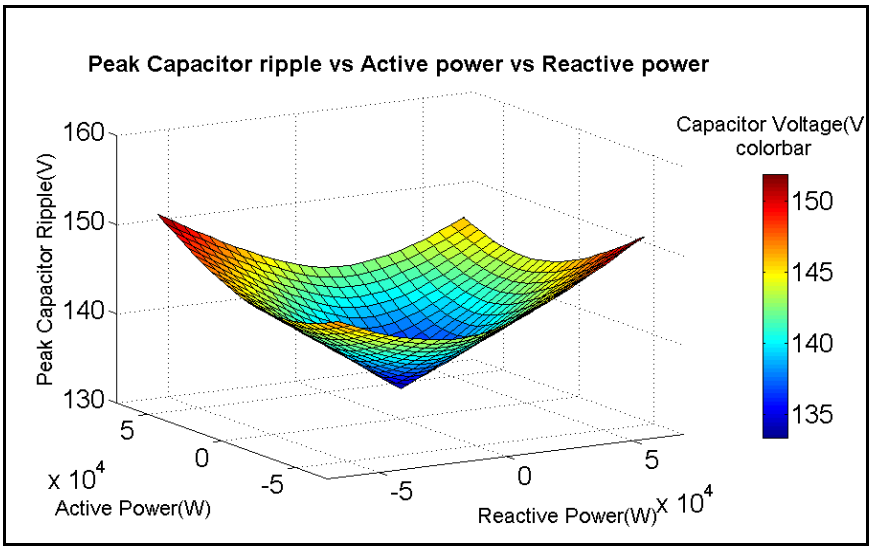

Figure 5.9 Capacitor peak voltage as a function of Active and Reactive Power

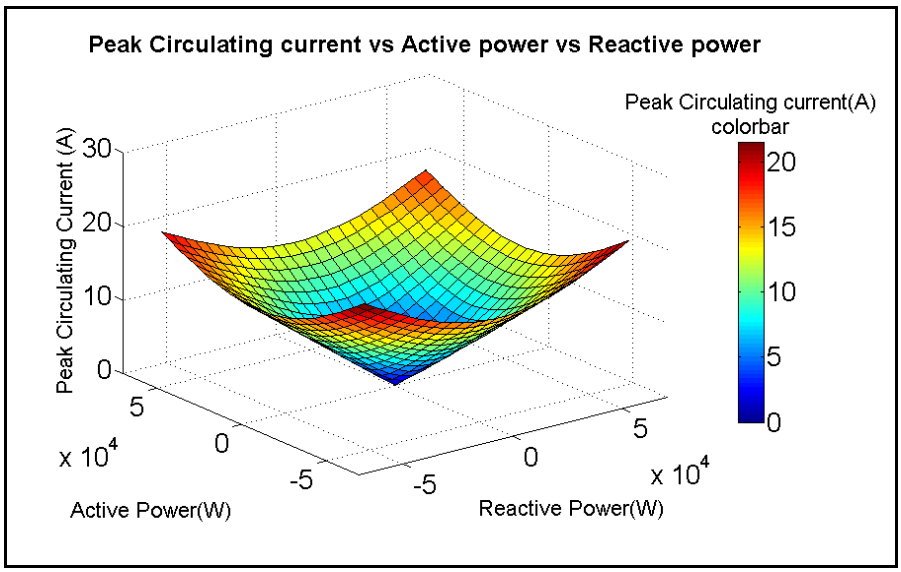

Figure 5.10 Circulating current peak value as a function of Active and Reactive Power

The results from Figure 5.9 and 5.10 give good estimation of how capacitor voltage and circulating current peak changes as a function of active/reactive powers. Knowing the operating region of these key system parameters can allow optimization of MMC system design process.

5.2 EXTENSION OF MMC OPERATING REGION DURING NON-IDEAL SUPPLY CONDITIONS

As discussed in the previous chapter, during unbalance supply conditions the active and reactive powers can be maintained constant using CPC control structure but the DC side power is reduced due to the increase in converter losses (only inductor copper loss was considered in simulation). The converter loss percentage is higher during unbalance condition compared to balance condition. This is due to the fact that during unbalance condition the faulted phase(s) contributes lower amount in total dc current but it still needs to provide significant amount of supply phase current in order to maintain three-phase current symmetry on ac side. Therefore the copper losses, conduction losses and switching losses are unavoidable for the phase legs under fault. To understand the effect of losses on converter performance during balance and unbalance supply conditions it is necessary to investigate into converter loss modeling. This dissertation proposes a simple method for estimating converter losses. This method can also be implemented during runtime to estimate instantaneous losses and can help to extend operating limits of MMC during unbalance supply condition. This method and its applications are discussed in following sections.

5.2.1 SIMPLIFIED LOSS MODEL DEVELOPMENT

A loss model of MMC can be built using power loss equations and some datasheet parameters of the semiconductor devices used in MMC system. A half-bridge MMC has 2 IGBTs and 2 diodes in every sub-module. Therefore it is necessary to find

switching and conduction losses associated with both transistors and diodes. The basic equations of switching and conduction loss are shown below.

IGBT Turn-on loss:

$$P_{on\_T} = I_{avg\_T} * K_{on} \tag{5.15}$$

IGBT Turn-off loss:

$$P_{off\_T} = I_{avg\_T} * K_{off} \tag{5.16}$$

Diode Reverse-Recovery loss:

$$P_{rr\_D} = I_{avg\_D} * K_{rr} \tag{5.17}$$

IGBT Conduction loss:

$$P_{cond\_T} = I_{avg\_T} * V_{CE0} + {I_{rms\_T}}^2 * R_{CE} \tag{5.18}$$

Diode Conduction loss:

$$P_{cond\_D} = I_{avg\_D} * V_{D0} + {I_{rms\_D}}^2 * R_D \tag{5.19}$$

Arm copper loss:

$$P_{copper} = {I_{rms\_arm}}^2 * R_o \tag{5.20}$$

Where,

I_{avg_T} & I_{avg_D} are Average currents through IGBT and Diode respectively

I_{rms_T} & I_{rms_D} are RMS currents through IGBT and diode respectively

K_{on} is slope of IGBT turn-on energy loss calculated from datasheet

K_{off} is slope of IGBT turn-off energy loss calculated from datasheet

K_{rr} is slope of Diode reverse-recovery energy loss calculated from datasheet

V_{CE0} is IGBT collector to emitter voltage drop at zero current

V_{D0} is Diode forward voltage drop at zero current

R_{CE} is IGBT collector to emitter resistance during on state

R_D is Diode forward resistance during on state

Computation of $K_{on}, K_{off}, K_{rr}, V_{CE0}, V_{D0}, R_{CE}$ & R_D is done using datasheet parameters and the procedure used is explained in Appendix C.

Using these equations a good estimate on switching and conduction losses for both IGBTs and Diodes in a sub-module can be made. But, in order to achieve that it is necessary to compute Average and RMS currents flowing through each of these semiconductors. One way to calculate this loss is to use the arm current and instantaneous gate pulses of submodules. By knowing the instantaneous gate pulse logical value (0 or 1) and instantaneous arm current it is possible to determine which of the four semiconductor devices is conducting. Note that only one semiconductor device in a sub-module conducts at a time. This allows to find instantaneous currents through all the four semiconductors. Once the instantaneous current is known then average and RMS values of the currents flowing through that device can be found.

Figure 5.11 and Table 5.1 show which device conducts for a given combination of arm current direction and gate pulses.

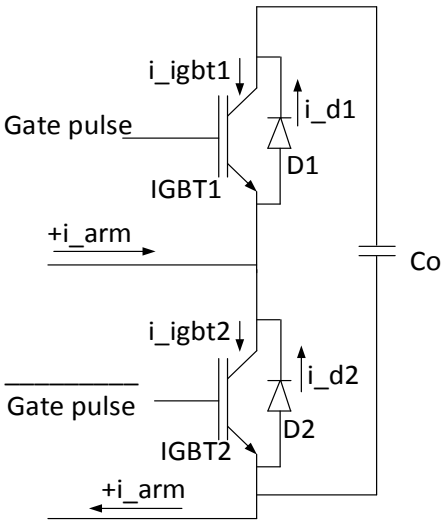

Figure 5.11 Various paths Arm current can take through a sub-module

Table 5.1 Separating sub-module current into individual semiconductor currents

Arm current direction	Gate pulse	ON semiconductor
+ve	0	IGBT2
+ve	1	Diode1
-ve	0	Diode2
-ve	1	IGBT1

Figure 5-12 shows the block diagram for computing Average and RMS currents.

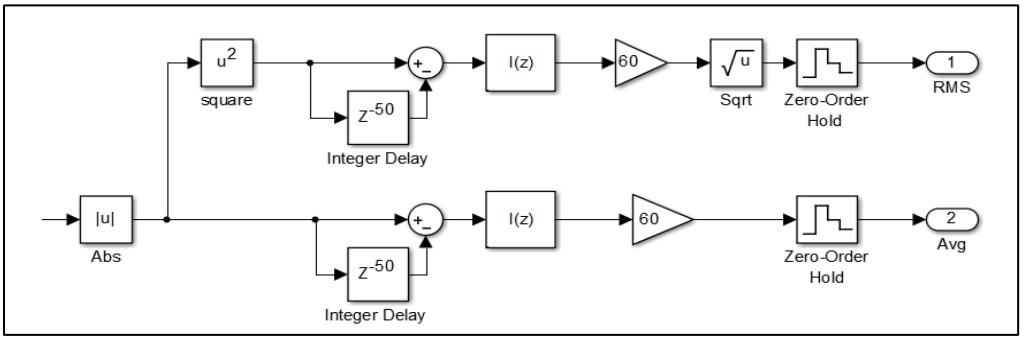

Figure 5.12 RMS and average current computation block diagram

Using above method, individual semiconductor currents are calculated and an example of such is given in Figure 5.13.The computed Average and RMS currents are then used to estimate both switching and conduction losses for each semiconductor device. Not that the Average and RMS currents are updated once every fundamental cycle of arm current.

Switching losses are computed every time the gate pulse toggles between 0 and 1. The possible switching transitions are shown in Table 5.2.

Table 5.2 Semiconductor switching transitions

Arm current direction	Gate pulse transition	Switching Transition
+ve	0 to 1	IGBT2 turns OFF
+ve	1 to 0	IGBT2 turn ON Diode1 turns OFF
-ve	0 to 1	IGBT1 turn ON Diode2 turns OFF
-ve	1 to 0	IGBT1 turns OFF

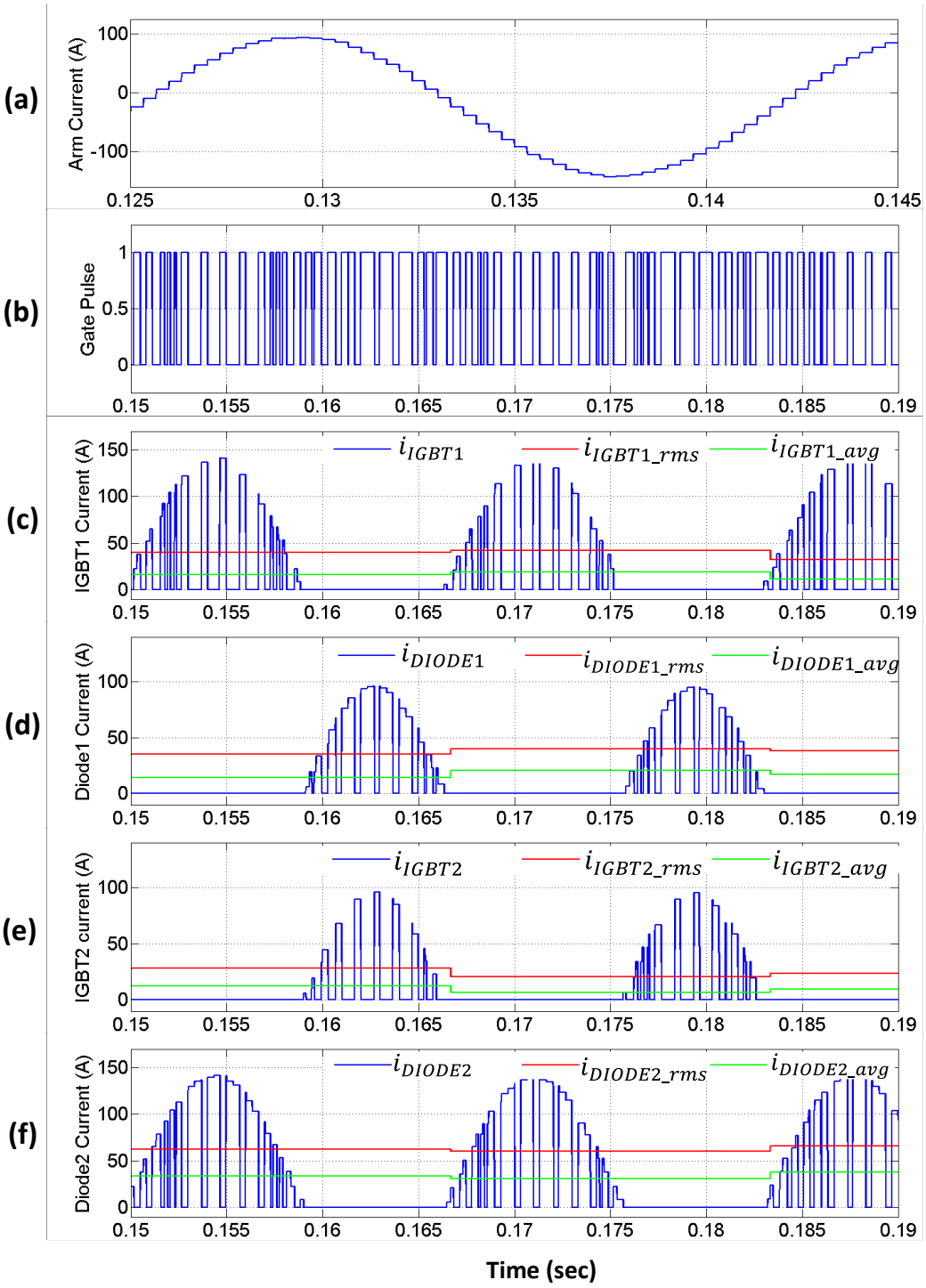

Figure 5.13 Extraction of individual semiconductor currents using arm current and sub-module gate pulse. (a) Arm current (b) sub-module gate pulse (c) IGBT1 current (d) Diode1 current (e) IGBT2 current (f) Diode2 current

Instantaneous switching loss is computed by using the instantaneous arm current and using the slopes K_{on}, K_{off} & K_{rr} which are found from datasheet. Once the energy

loss is known then the power loss can be easily computed. The conduction losses on the other hand are updated every time the average and RMS currents are updated, which is once per fundamental cycle of arm current.

Once the RMS and average currents are found as shown in Figure 5.13, then the power losses can be computed for the sub-modules in each arm. Figure 5.14 shows the power losses (switching +conduction) for six sub-modules in upper arm of phase leg A. Since all the sub-modules in an arm share the same arm current and the voltage across each sub-module (capacitor voltage) is also the same due to the voltage balancing algorithm (Figure 2.19) they all exhibit similar power loss in steady state. Due to this reason calculation of power loss for one sub-module in an arm is enough in order to minimize computational effort while still providing reasonable accuracy.

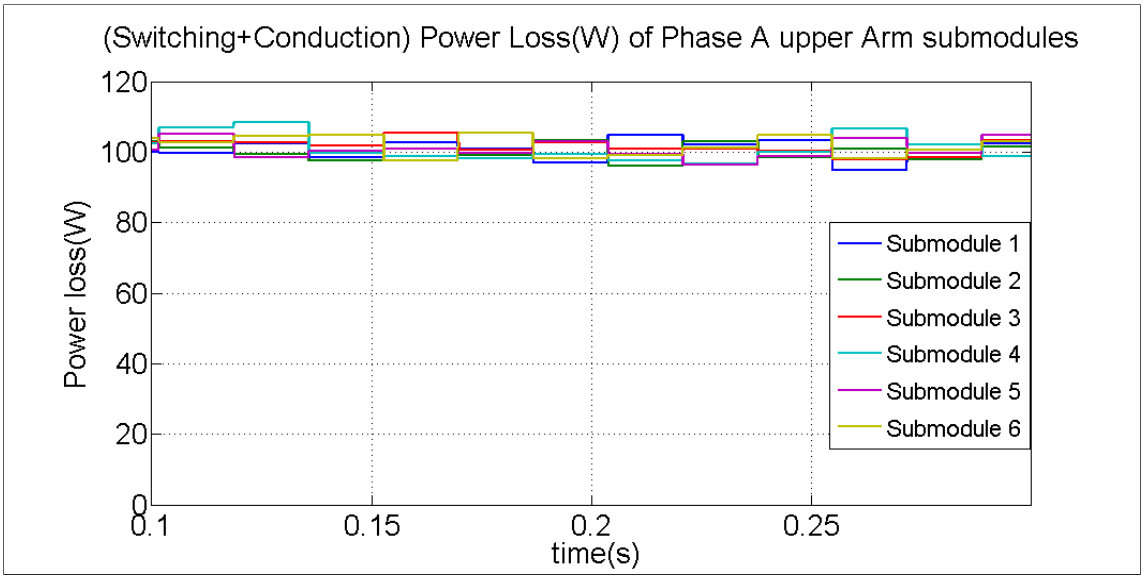

Figure 5.14 Power loss comparison of all sub-modules in an Arm

Using above results the switching loss, conduction loss are calculated for one sub-module in each arm and then multiplied by total number of sub-modules in one arm (which is six in this case). Then all the six arm's switching, conduction and copper losses are added together to get the total power loss in the system. This total power loss is then

subtracted from the active power in order to get better estimation of dc power. The results of above mentioned power loss calculation method are shown in Figure 5.15.

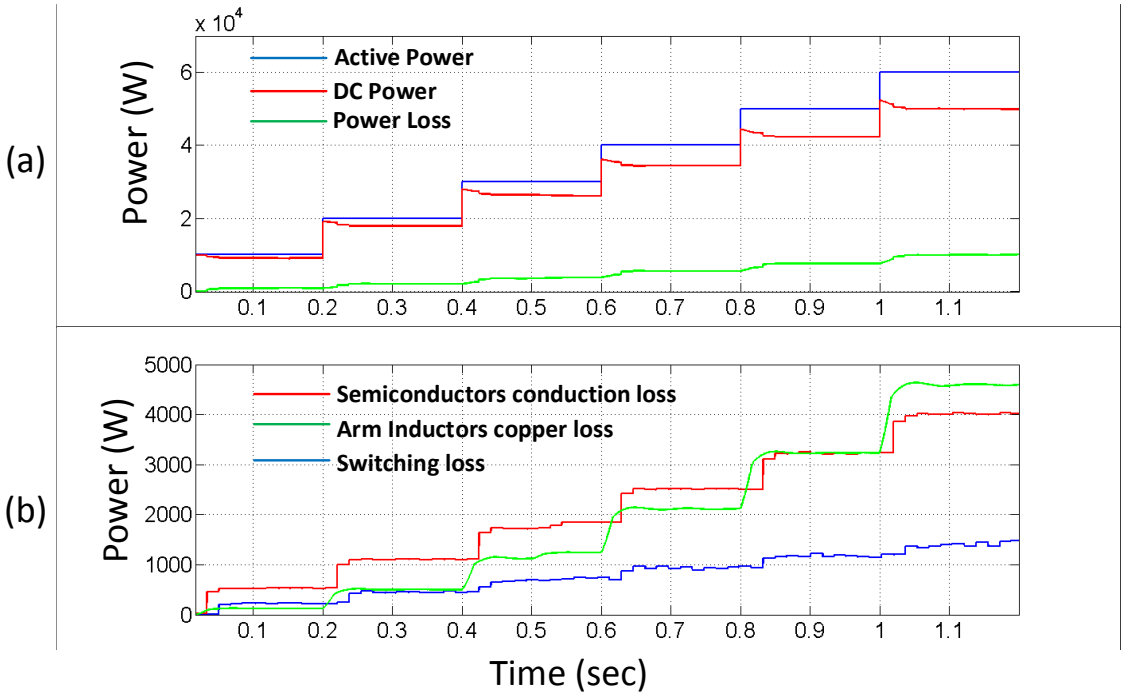

Figure 5.15 Powers under balance conditions (a) Active power, DC power and power loss (b) Total switching, conduction and copper losses

The run-time loss modelling discussed above is very useful in order to extend the operating limit of the MMC during unbalance supply conditions as explained in the following section.

5.2.2 DC POWER TRANSFER LIMIT UNDER UNBALANCE SUPPLY

As discussed in chapter 4 (Figure 4.15), keeping power reference constant during unbalance supply conditions is not feasible. This is due to the fact that, for faults the positive sequence voltage component magnitude is much smaller than the nominal value. If the power reference is kept constant during such conditions then the supply phase currents will increase in order to keep the active power constant. Increase in supply phase

currents above their maximum allowed limit will damage the active and passive elements in the system.

A simple solution for this problem was proposed in chapter 4 (Figure 4.19). In this method the power references (both active and reactive power) are made function of three-phase positive sequence voltage RMS value. This ensures that phase currents are kept under the limit for various unbalanced situations as shown in Figure 4.19, Figure 4.21 and Figure 4.23. These results are the best possible to achieve when the converter is operating at its maximum rated power. But when the converter is operating below its rated power then this method seems to limit the performance of system. This limitation is demonstrated in Figure 5.16 and Figure 5.17.

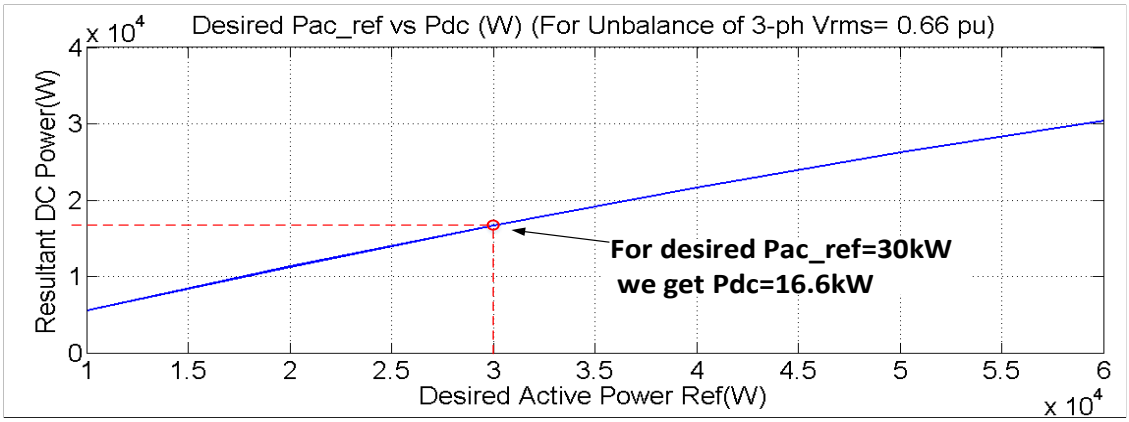

Figure 5.16 Power transfer using reference reduction method (from chapter 4).

In this case, for a particular unbalance supply (that gives three-phase RMS voltage of 0.66p.u.) the power conversion performance is plotted for different active power values. As seen from Figure 5.24, due to the unbalance condition the resulting dc side power is well below the desired power references. This is due to the reason that the desired ac power reference is reduced as a function of positive sequence voltage magnitude and therefore the dc power also reduces.

Consider a test case of Figure 5.17 where the converter is operating at half of its rated power (30kW). Then, during unbalance conditions this power will be further reduced to 20kW (proportional to positive sequence Vrms) and so will be the DC power. But doing this keeps the phase currents unchanged to maintain P=V*I relation. As seen from Figure 5.17 (b) during fault the phase currents are still below the maximum current limits of converter. The maximum possible supply phase current is what the converter needs to handle at rated power of 60kVA which is 235A peak. This means there is a possibility to increase the dc power to the desired value (or as much close as possible to the desired value) by letting the phase currents increased within their defined limits.

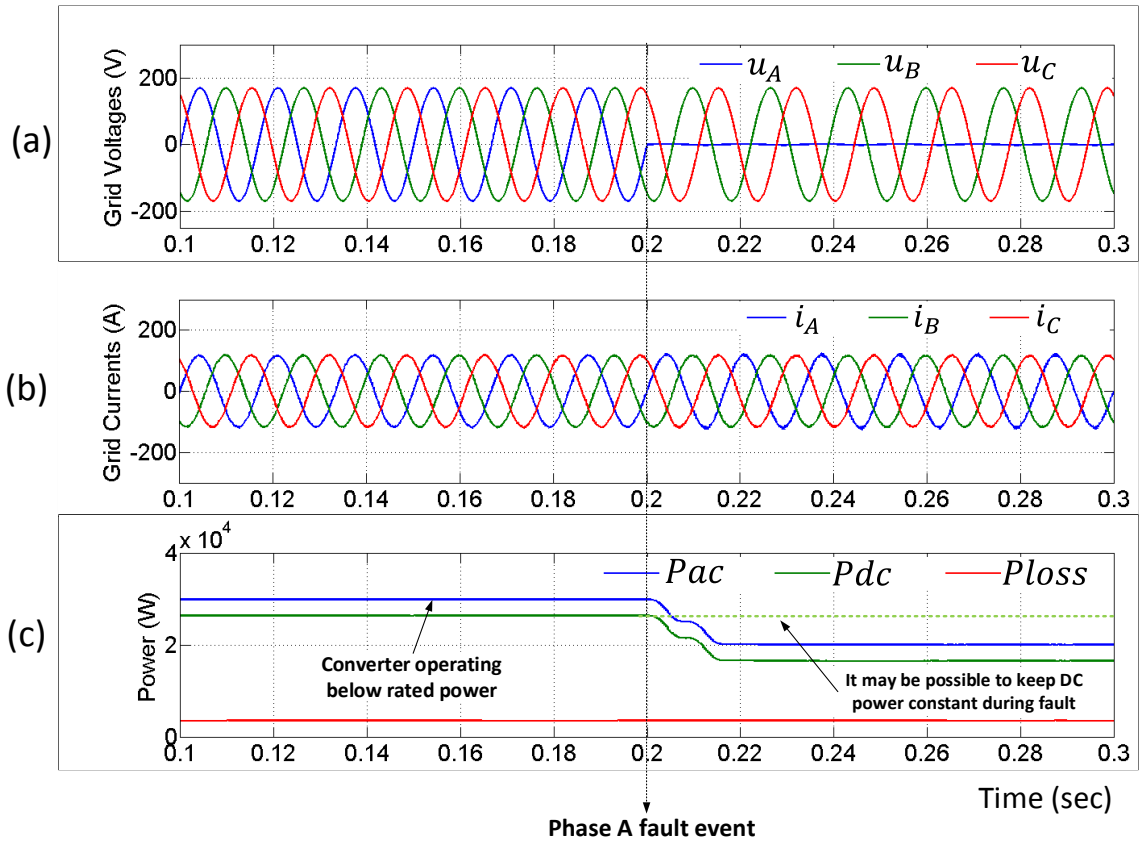

Figure 5.17 Converter operating below rated power during fault

It will not be possible to keep dc power constant all the time (depends on power reference, fault severity and other system limits) but by effectively using a system's maximum power dissipation capacity, the system's ability to work at the best possible operating point under any unbalance supply conditions can be certainly increased. A novel method to achieve this goal is presented in the following section.

5.2.3 Extending the DC power transfer limit

Extension of dc power transfer limit during unbalance supply conditions can be accomplished by increasing active power reference until desired dc power is achieved or until system reaches to its maximum possible power dissipation capacity, the latter being most important one. A converter system is designed to dissipate certain amount of loss at rated power using heat-sink, liquid or air cooling mechanism etc. Under no condition this power dissipation limit should be exceeded. Although the active devices has maximum current limit, excessive power loss due to switching and conduction losses can cause degrading or destruction of the device. This can occur even if the device current is below its maximum current limit. For presented MMC design the maximum power loss could be 10kW at full rated power of 60kW based on Figure 5.15 (a). The power loss modeling as discussed earlier in this chapter can now be used to extend the operating limits of MMC. There are two ways to modify the active power reference which are discussed in following section.

5.2.3.1 USING MEASURED DC POWER AS FEEDBACK

The dc power is obtained by multiplying instantaneous dc bus voltage and dc bus current. Although the dc bus voltage is fairly constant (mainly due to phase leg capacitors) the dc bus current on the other hand is not as smooth. Due to the switching harmonics and low frequency non-periodic harmonics introduced by circulating current controller into the dc bus current, it cannot be directly used to compute dc power. Note that, the attempt is to modify active power reference value which should be as constant as possible in steady-state. The active power controller is designed for very low crossover frequency (3 Hz) in order to avoid interference with current control loop. Therefore, the dc power with switching and low frequency harmonics cannot be directly interfaced with the active power reference modification method. One solution is to compute RMS value of dc current and then compute the DC power. The block diagram to modify active power reference using dc current is shown in Figure 5.18.

This algorithm updates active power reference value once per switching event. This is the fastest the modulating signal can be updated in the hardware system. The flow chart in Figure 5.18 explains how the active power reference is increased or decreased based on resultant dc power and/or instantaneous system losses. The result of implementing this algorithm is shown in Figure 5.19.

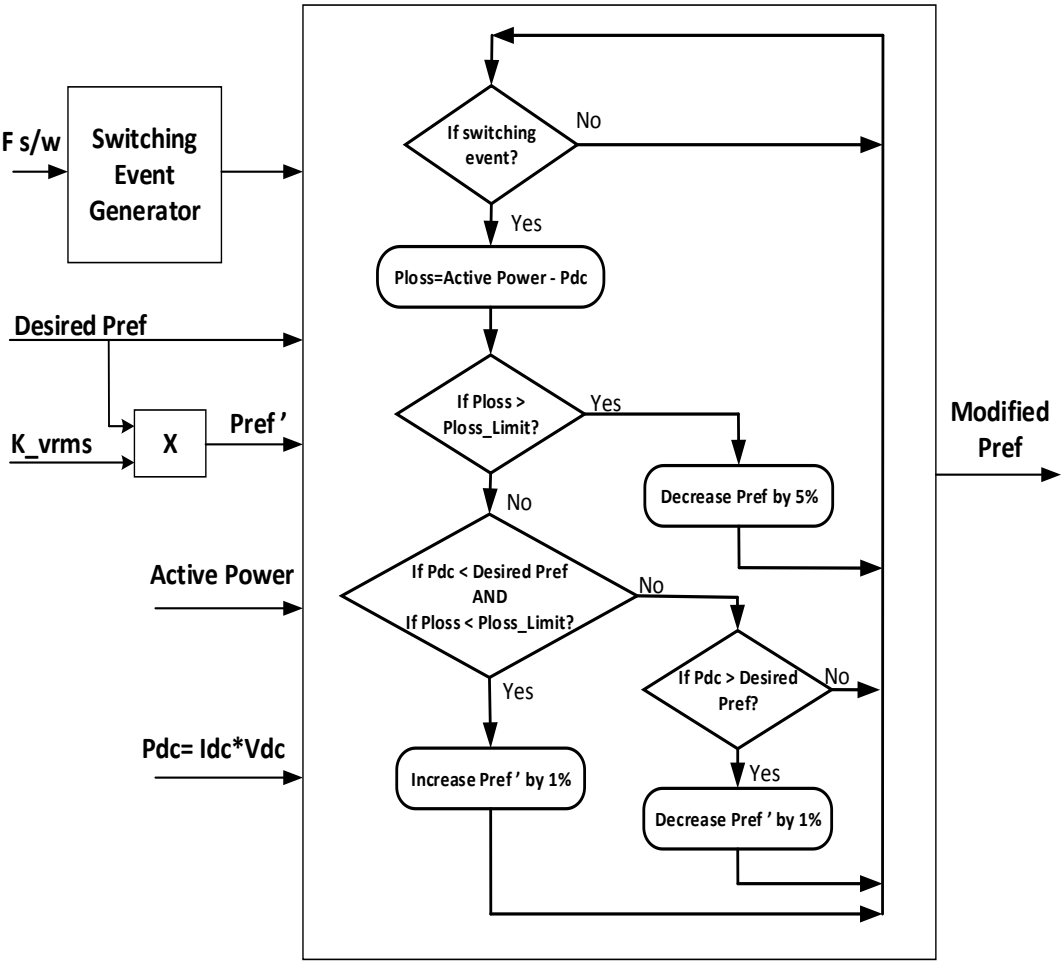

Figure 5.18 Power reference modification algorithm (using DC current RMS value)

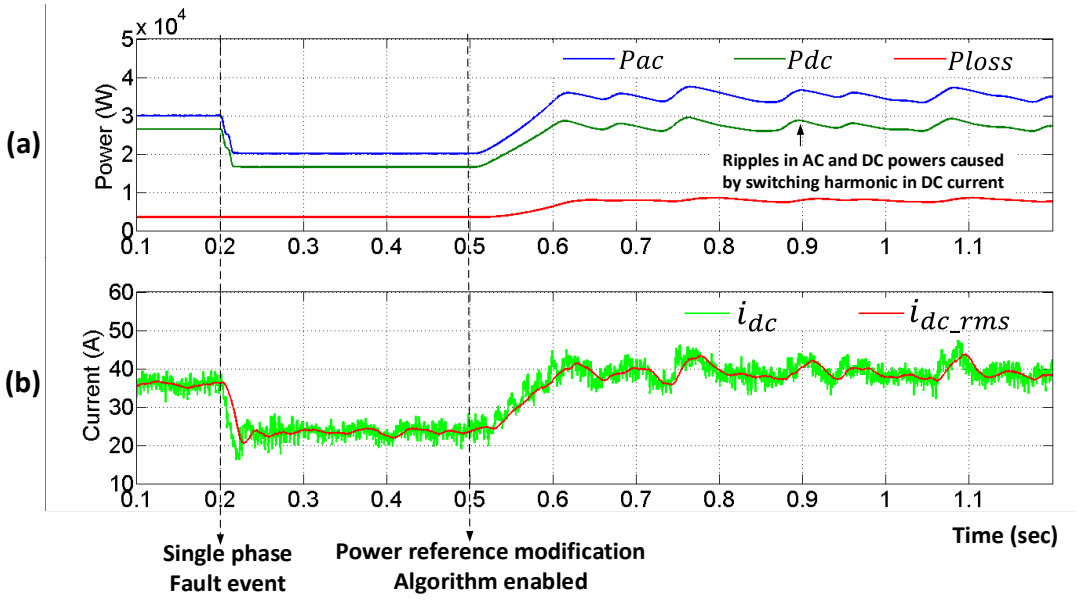

Figure 5.19 Performance of power reference modification algorithm (using DC current)

In Figure 5.19, the converter is operated at half the rated power prior to fault event (at t=0.2sec). After the fault event the active power reference is reduced (same method as in Figure 4.19 (e) and converter has new steady state with reduced active and dc powers. At 0.5sec the algorithm from Figure 5.18 is enabled to modify the active power reference in order to increase the dc power to its desired value. The active and dc powers do increase but they have low frequency oscillations in steady-state. This is due to the fact that even the RMS value of dc current is not stable enough to produce a stable feedback. Any oscillations in RMS dc current will cause further oscillations in active power reference which will cause oscillations in dc current and the process will repeat. This oscillatory feedback can also cause instability in system during transients. Therefore this method cannot be used to modify the active power reference value.

5.2.3.2 USING COMPUTED POWER LOSS AS FEEDBACK

The block diagram for this method is shown in Figure 5.20. From Figure 5.15 it is observed that the computed losses are not affected by switching and low frequency harmonics and therefore has very low ripple as compared to instantaneous or RMS dc power. Therefore, the simplified loss model can be used in the power modifying algorithm.

Figure 5.20 is logically similar to Figure 5.18 except that the dc current feedback is replaced with power loss as a feedback and then the dc power is computed by subtracting power loss from active power. The results for this method are shown in Figure 5.21.

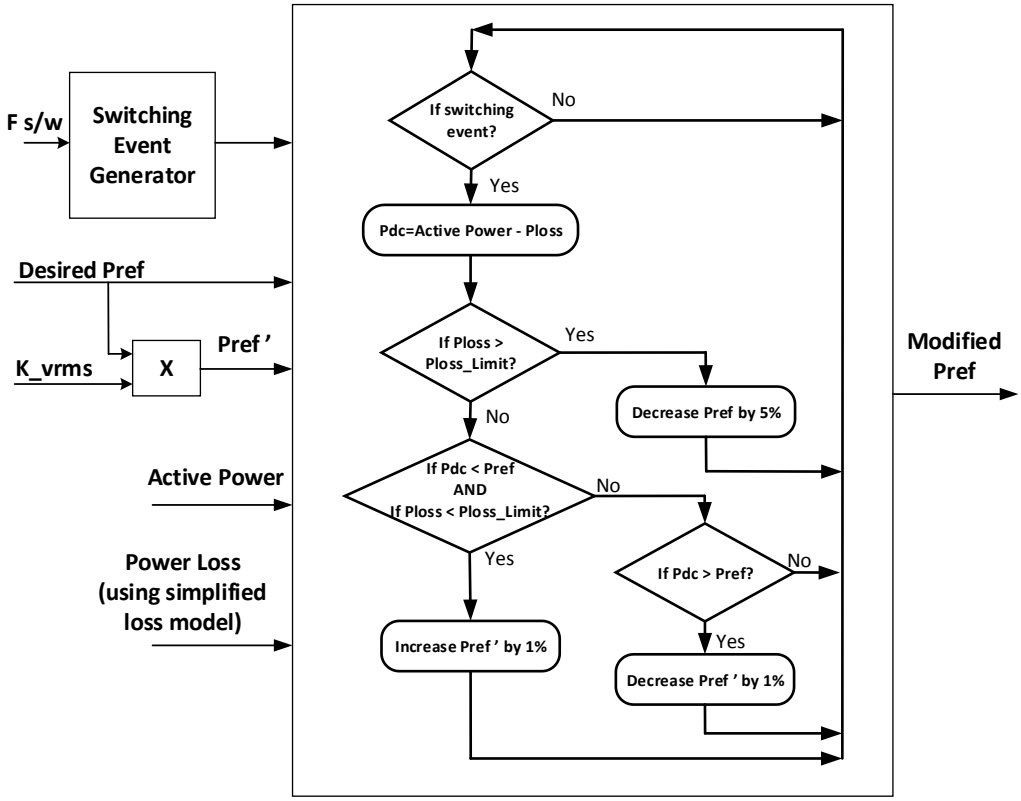

Figure 5.20 Power reference modification algorithm (using simplified Loss model)

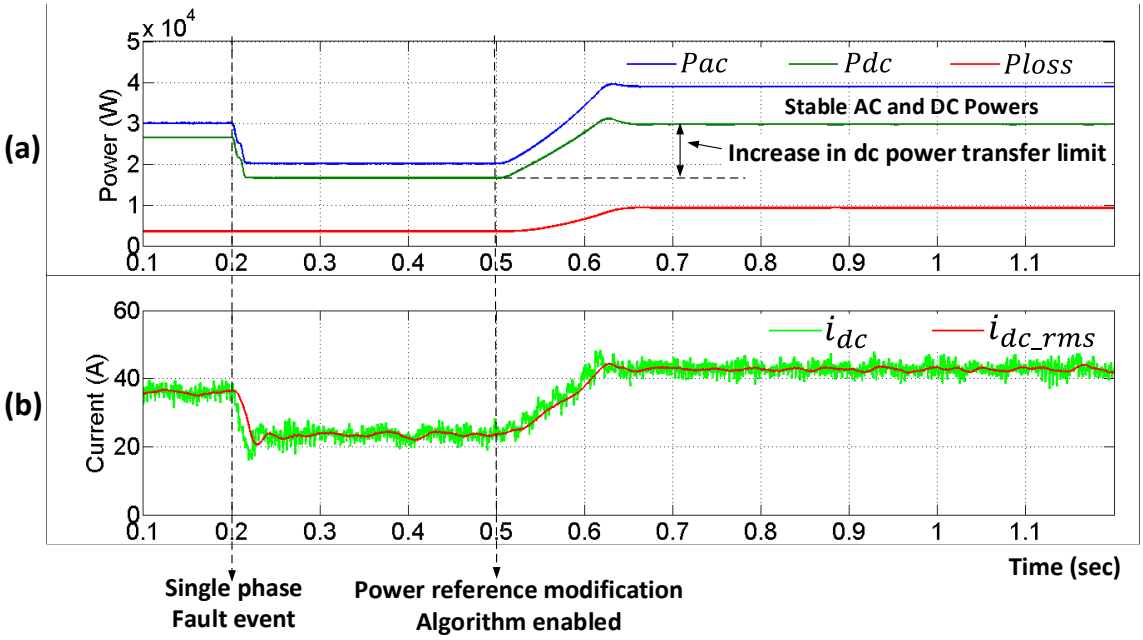

Figure 5.21 Performance of power reference modification algorithm (using Loss model)

Fault event and algorithm (from Figure 5.20) enabling events are similar to Figure 5.19. From Figure 5.21 (a) it can be seen that the algorithm successfully modifies active power reference such that the dc power meets desired power ref and while doing that the power loss does not exceed 10kW limit, which is rated power loss dissipation capacity for designed MMC. The active and dc powers have negligible ripple in steady state. This method is further validated under phase-to-phase faults and two-phase to ground fault. The desired dc power in this test is 30kW. The results of this test are shown in Figure 5.22.

Figure 5.22 shows that during phase-phase fault the algorithm is able to raise the dc power to the desired value of 30kW while during two-phases to ground fault the positive sequence voltage RMS value decreases significantly which causes to increase losses rapidly even for low power transfer to dc side and therefore when dc power reaches 18kW the power losses hit 10kW limit and the algorithm successfully stops further increase in active power reference and steady-state is reached.

A comparison of resultant dc power using reference reduction method from chapter 4 and reference modification using power loss method is shown in Figure 5.23.

Using first method (from chapter 4) the power reference is reduced as a function of positive sequence voltage component of grid voltage. This method cannot be used to achieve desired power reference during unbalance condition. Whereas, using second method the best possible operating point for power reference is generated by algorithm of Figure 5.20 which allows to achieve desired power references under many unbalance supply conditions.

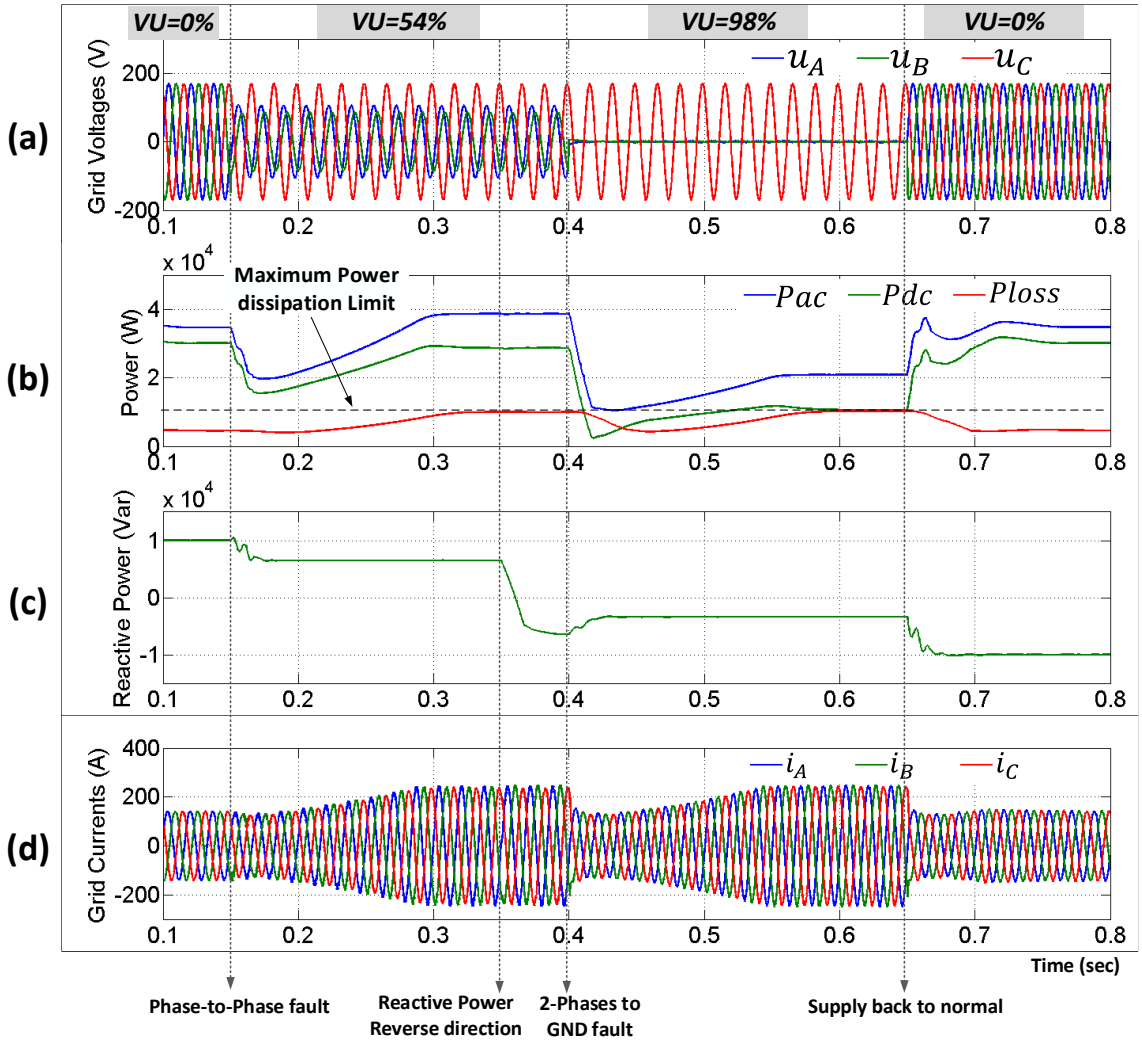

Figure 5.22 Performance of proposed method to extend the dc power transfer limit during unbalance supply

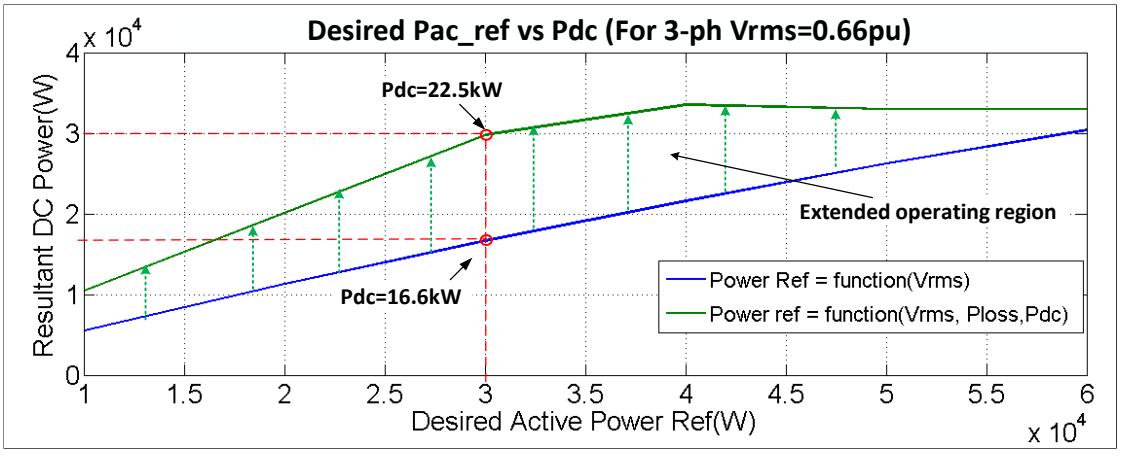

Figure 5.23 Comparison of two power reference modification methods during unbalance

Based on this loss calculation method power losses for various types of unbalance supply conditions can be obtained. Figure 5.24 shows comparison between two methods of active power reference modification under various asymmetric supply conditions. In method 1 the power reference is function of three-phase positive sequence voltage RMS value whereas in method 2 active power reference is function of three-phase positive sequence voltage RMS value, run-time loss and DC side power.

Figure 5.24 (a) shows that in method 1 the resultant dc power is linear function of supply asymmetry whereas (b) shows that under all unbalance test conditions the resultant dc power is linear function of asymmetry in some region and then saturated as the power reference is further increased. In Figure 5.24 (b) and (d) the saturation that happens in each test case indicates that the power loss maximum limit has reached and further increase in desired power reference will not increase dc power but will keep it constant to that level.

Figure 5.24 (c) shows that since the power reference is always proportional to the supply asymmetry the power loss for all unbalance test cases should be same.

As voltage asymmetry increases the phase leg(s) under fault needs more and more energy from other phases to keep their capacitors charged to the nominal value and also generate sinusoidal phase currents. Therefore as voltage asymmetry becomes severe the system suffers higher power losses even for lower amount of power transfer. Figure 5.24 (e) shows the system's efficiency as a function of unbalance test cases.

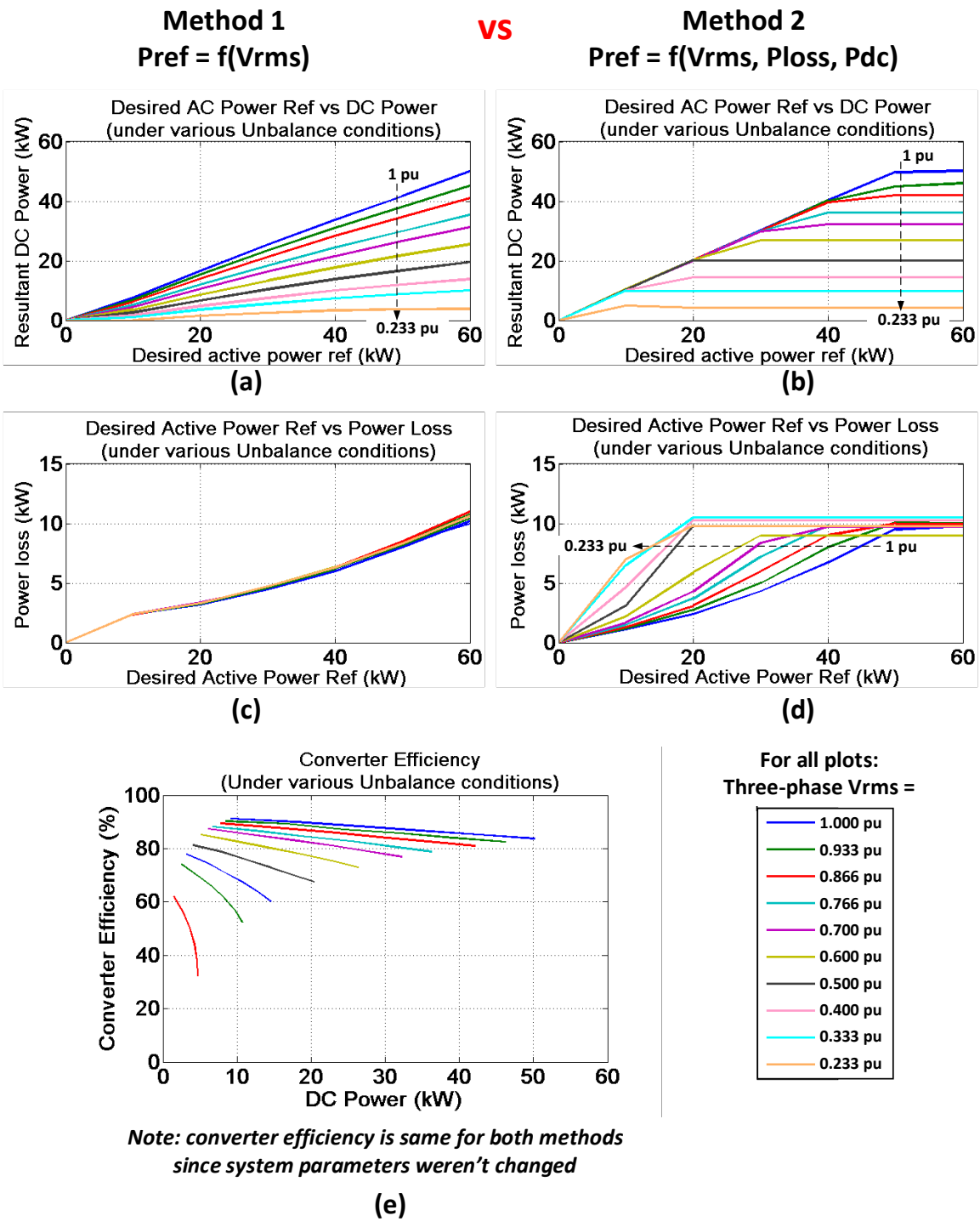

Figure 5.24 Comparison of performance of two active power reference modification methods for various unbalance test cases

The results obtained so far are for two reference modification methods. Similar results are obtained for the case where the power reference is always fixed regardless of the unbalance supply condition. All these results are then plotted in more intuitive way (surface plots) in order to obtain better understanding of how operating region of MMC is affected by different reference calculation methods. The results are shown in Figure 5.25 and Figure 5.26.

Figure 5.25 shows the DC power transfer capability of three different reference calculation methods. In Plot (a) the reference is fixed therefore it supplies maximum possible power to the dc side. Plot (b) shows that the power reference is modified as a function of three-phase positive sequence RMS voltage (Vrms) therefore the DC power also decreases as a linear function of Vrms. Plot (c) on the other hand has properties of both plot (a) and (b). Corresponding power loss vs desired power reference and Vrms is shown in Figure 5.26.

Figure 5.26 (a) has unfeasible power losses if the active power reference is kept fixed during the unbalance conditions. Figure 5.26 (b) shows that for a given desired power reference the losses are constant during various unbalance conditions which means the DC power has to decrease accordingly (as seen from Figure 5.25 (b). Whereas, plot (c) shows that this method utilizes system's power dissipation capacity to its maximum potential. From Figure 5.25 (c) and Figure 5.26 (c), it can be observed that under all the tested unbalance conditions some of the operating region of MMC achieves the desired power on dc side while remaining region operates at maximum power loss dissipation.

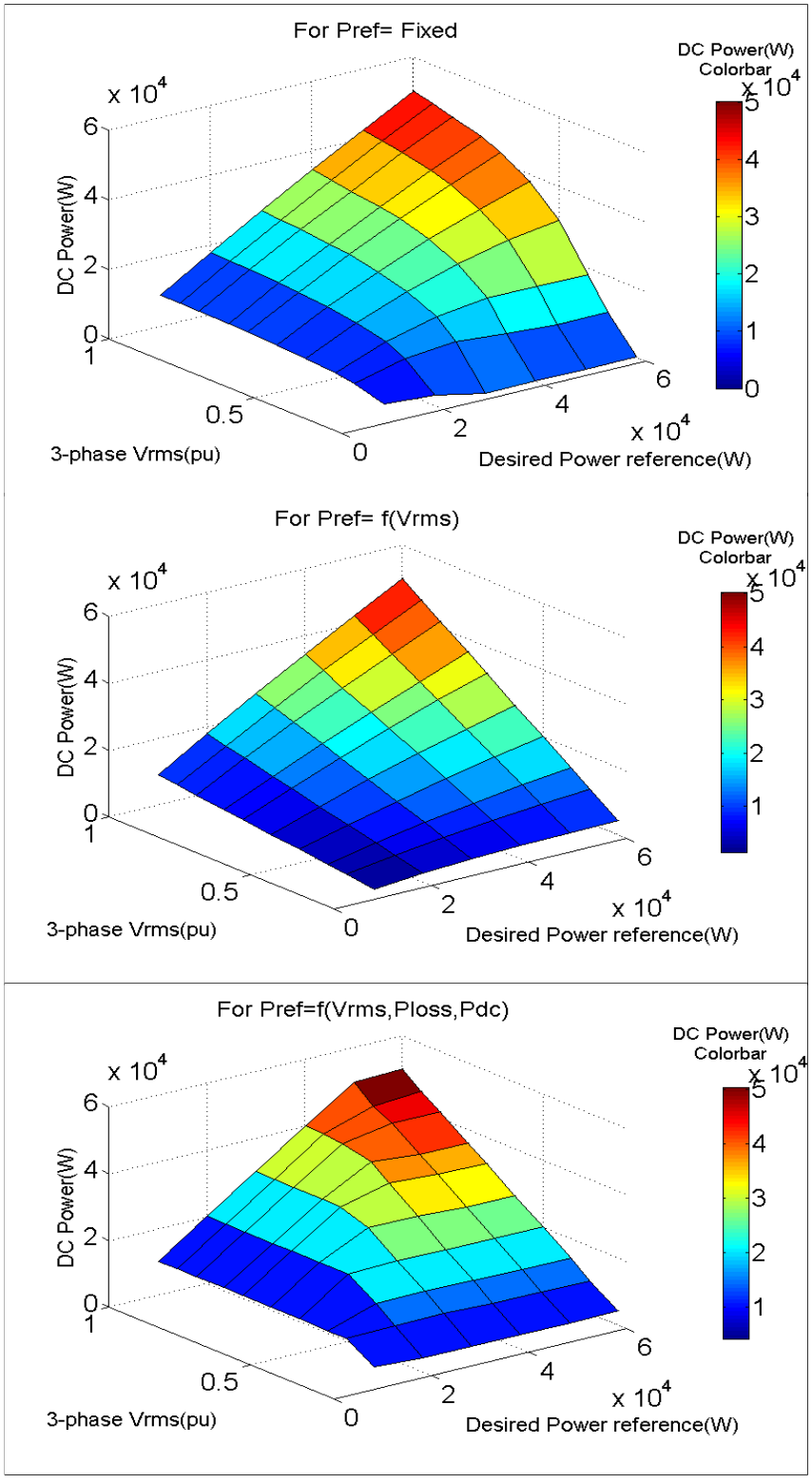

Figure 5.25 DC Power vs Desired Power Ref vs supply unbalance for three Ref calculation methods

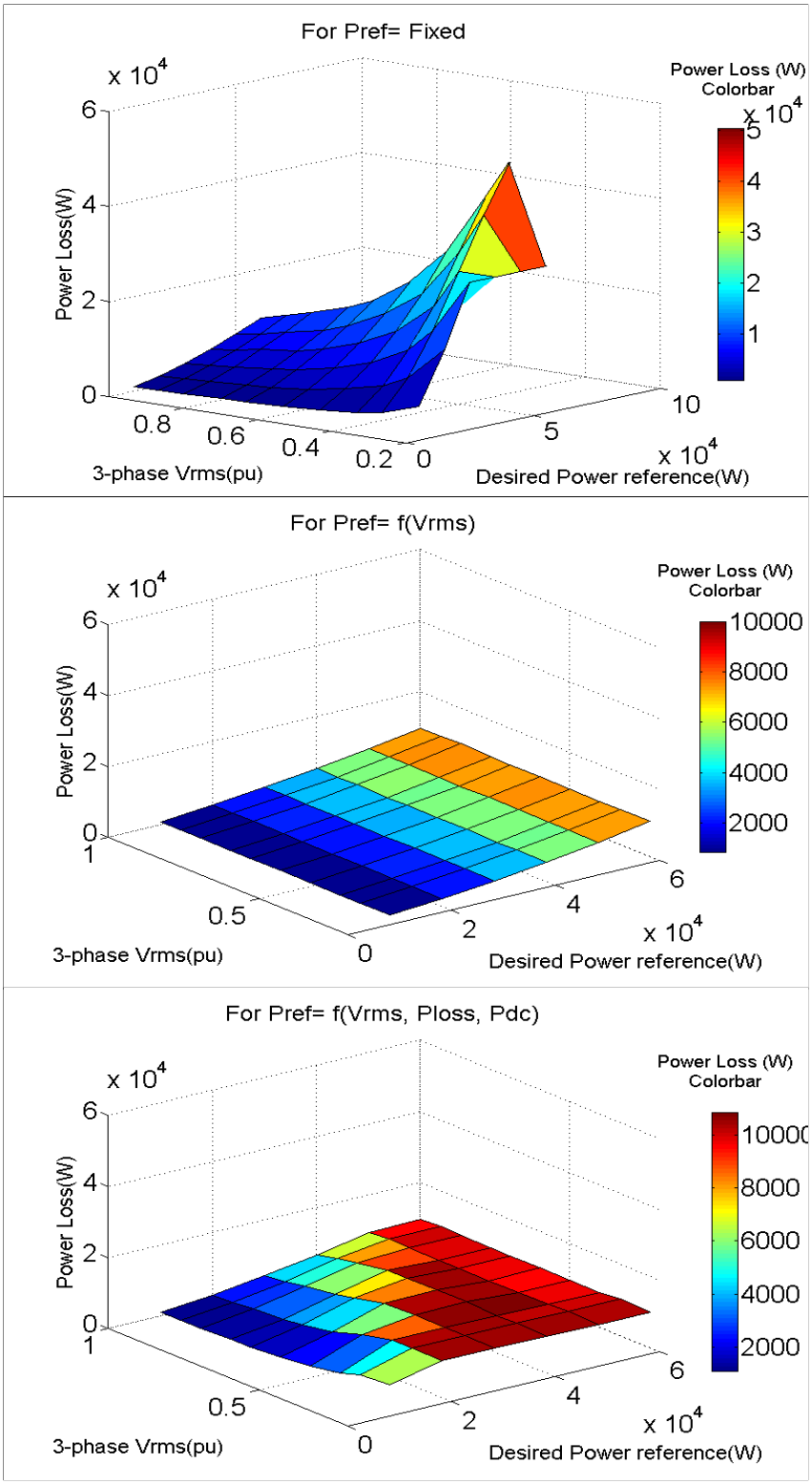

Figure 5.26 Power Loss vs Desired Power Ref vs supply unbalance for three Ref calculation methods

Based on the above results for different unbalance supply test cases it can be concluded that the operating limits of a MMC during non-ideal supply conditions can be successfully extended using proposed reference modification method without exceeding systems thresholds such as device voltage ratings, current ratings and thermal dissipation limits.

CHAPTER 6

CONCLUSION AND FUTURE WORK

This dissertation presents a new control method for double star type Modular Multilevel Converters, used in utility applications, that enables correct operation under non-ideal conditions on the AC side of the converter.

A detailed mathematical model of a MMC was developed that provides insight into the relations between supply currents, circulating currents and converter voltages. Based on a literature study a commonly used MMC control system, that implements conventional voltage balancing algorithm, phase-shifted carrier modulation, outer power controllers, and synchronous frame PI controllers based inner phase current and circulating current controllers was developed as a baseline system. The performance of the baseline MMC control system was studied under both balanced and unbalanced AC supply conditions. It was observed that during unbalance AC supply the conventional control system is not capable of maintaining the desired performance of the MMC.

A new control method based on a frequency domain approach with an appropriate orthogonal current decomposition was developed. In this method, by extracting fundamental frequency component and performing symmetric component decomposition of grid voltages it is possible to generate symmetric sinusoidal supply currents under phase-to-phase faults, single phase-to-ground fault, two phases-to-ground fault and non-sinusoidal supply conditions. The proposed controller ensures that only positive sequence

currents are injected into the grid. A simple method for modifying active power reference as a function of three-phase voltage RMS value during asymmetric condition was suggested. This method ensures that the supply currents and sub-module capacitor voltages do not exceed their constraints during asymmetric supply condition. A new circulating current controller based on frequency domain decomposition of arm currents was also presented which minimizes circulating currents, maintains average voltage across each sub-module capacitor at its nominal value and also reduces dc bus current ripples during asymmetric supply conditions. The proposed control structure assures that ripple free powers are generated on both ac and dc sides during supply asymmetry.

Typical MMC average models either assume submodule capacitors as ideal voltage sources (this gives an ideal modulated staircase waveform across each arm) or assume an entire arm as a controlled voltage. In both cases it is not possible to predict either the capacitor voltage ripples or the circulating current magnitudes. Therefore a new average model of a MMC based on linearly varying arm capacitance and its voltage, both as a function of modulating signal, was presented. This average model preserves the dynamics of arm inserted capacitance while the effect of switching frequency and voltage unbalance is neglected. Therefore, it allows quick calculation of submodule capacitor voltage and circulating current magnitudes as a function of desired input voltage and power references. By knowing the estimated operating region using the proposed average model and constraints on the system parameters, the operating region of MMC can be extended under certain power references and asymmetric supply conditions.

In order to extend the maximum possible power transfer capability of a MMC under non-ideal AC supply condition a simplified run-time loss modeling method and a

power reference computation algorithm was presented. The loss model provides a run-time total loss feedback to the power reference computation algorithm. The algorithm then computes the maximum possible power that can be exchanged between AC and DC systems without exceeding systems thresholds (such as semiconductor current limits, system's power dissipation capability etc.). The proposed loss model based power reference modification scheme was shown to extend the operating region of MMC as compared to the initial control structure presented in Chapter 4.

The presented operating region analysis of MMC assumes an average model and estimates parameter behavior as a function of system inputs only (grid voltages and power references). The scope of operating region analysis can be increased by incorporating the effects of submodule capacitance, arm inductance, device switching frequency and number of submodules in an arm (i.e. MMC level). Such an operating region analysis method will provide more valuable information to the MMC system design process. The operating region extension method presented in this dissertation is based on the comparison of certain system parameters and then modifying the power references. This method takes about ten fundamental cycles to reach steady-state and also cannot achieve zero steady-state error. Therefore there is a scope to improve the performance of this method in future work by using either a proportional integral controller which operates above power control loop or the power controller itself can be modified to include the reference modification algorithm.

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APPENDIX A

DESIGN OF TRADITIONAL CONTROLLERS

A.1 PHASE CURRENT CONTROLLER DESIGN

By using the block diagram of Figure 2.9 the equation for open loop transfer function of the current control loop is given by,

$$G_{OL}(s) = \left(Kp + \frac{Ki}{s}\right).\left(\frac{1}{Cpk}.\frac{1 - s.\frac{Ts}{4}}{1 + s.\frac{Ts}{4}}\right).\left(\frac{2Vdc}{Ro + s.Lo}\right) \qquad \text{(A.1)}$$

The values of controller gains Kp & Ki can be found by solving equation (A.1) at desired gain crossover frequency (w_c) to achieve desired phase margin At gain crossover frequency the gain of open loop transfer function is equal to 0dB i.e. the magnitude of equation (A.1) is equal to one. Using this criterion the equations for determining controller gains are given in equation (A.2) and (A.3).

$$\frac{Ki}{Kp} = \frac{wc}{\tan(-\frac{pi}{2} + PMrad + 2.tan^{-1}\left(\frac{wc.Ts}{4}\right) + tan^{-1}(\frac{wc.Lo}{Ro}))} \qquad \text{(A.2)}$$

$$Kp = Cpk.\frac{Ro}{2.Vdc}.\sqrt{\frac{1+(\frac{wc.Lo}{Ro})^2}{1+(\frac{Ki}{wc.Kp})^2}} \quad \text{(A.3)}$$

where, w_c is gain crossover frequency of open loop transfer function and PM is phase margin at w_c.

Using these equations the controller gains can be determined for desired system parameters. The desired system parameters are given below:

Sub-module switching frequency = 500Hz. This gives total switching frequency across one arm as, 500*Total number of sub-modules in an arm = 500*6 = 3000Hz.

Therefore, for single update Digital PWM F_{sw}= 3000Hz and $F_{samp} = F_{sw}$

$T_{samp} = T_s = \frac{1}{F_{sw}}$

Selecting open loop gain crossover frequency one order below switching frequency,

w_c =300Hz = 1884.5rad/s

Phase margin is selected to be PM=60deg in order to provide optimum trade-off between output oscillations and settling time.

Ro = 0.1 Ohm, Lo = 1mH and Vdc = 800V.

For above parameters the values of controller gains are found to be,

Kp = 0.91 and Ki = 465.

Open loop transfer function: (measured between point A and B in Figure 2.9)

$$G_{OL}(s) = \frac{-0.002429s^2 + 27.91\,s + 1.49e04}{1.333e-06s^3 + 0.01613s^2 + 1.6\,s} \quad \text{(A.4)}$$

Bode plot for this open loop transfer function with PI controller is shown in Figure A.1.

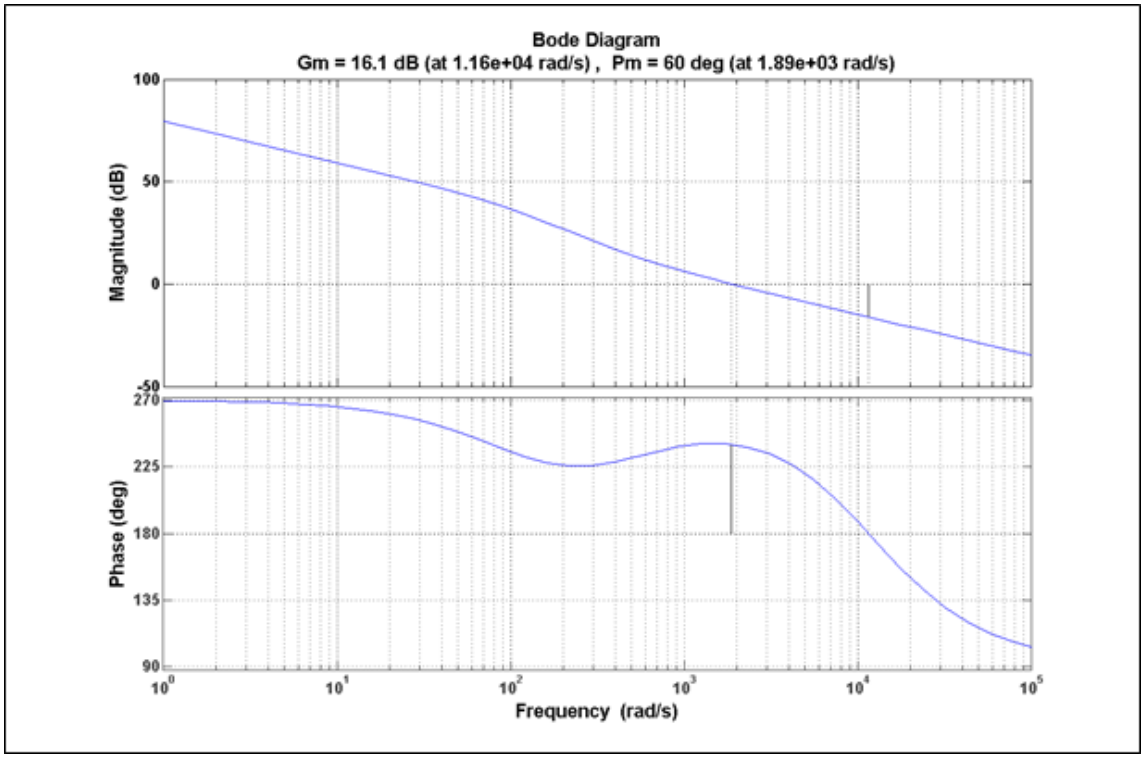

Figure A.1 Bode plot of traditional phase current controller open loop TF

Close loop transfer function:

$$G_{CL}(s) = \frac{-3.239\text{e}-09s^5 - 1.98\text{e}-06s^4 + 0.4662s^3 + 285.2s^2 + 2.38\text{e}04\ \text{s}}{1.778\text{e}-12s^6 + 3.972\text{e}-08s^5 + 0.0002626s^4 + 0.5178s^3 + 287.7s^2 + 2.38\text{e}04\ \text{s}} \quad \text{(A.5)}$$

Neglecting some very small coefficient terms from equation (A.5),

$$G_{CL}(s) = \frac{0.466s^3 + 285.2s^2 + 2.38\text{e}04\ \text{s}}{0.0002626s^4 + 0.5178s^3 + 287.7s^2 + 2.38\text{e}04\ \text{s}} \quad \text{(A.6)}$$

The locations of poles and zeros of closed loop current controller (equation (A.6)) are given as below,

$$P1 = -935$$
$$P2 = -935$$
$$P3 = -100.03$$
$$Z1 = -511.74$$
$$Z2 = -100.01$$

All the zeros and poles of current control closed loop are negative meaning they lie in left half plane of s-plane. Using Nyquist criteria this indicates that the closed loop system is stable.

A.2 POWER CONTROLLER DESIGN

By using the block diagram of Figure 2.11 & 2.12 equation for open loop transfer function of the power control loop between points A and B can be written as,

$$G_{OL}(s) = \left(Kp + \frac{Ki}{s}\right).(eqn\ (1.19)).\left(\frac{3Vph}{2}\right) \tag{A.7}$$

The values of controller gains Kp & Ki can be found by solving equation (A.7) at desired gain crossover frequency (w_c) to achieve desired phase margin At gain crossover frequency the gain of *o*pen loop transfer function is equal to 0dB i.e. the magnitude of equation (A.7) is equal to one. Using this criterion the equations for determining controller gains are given in equation (A.8) and (A.9).

$$\frac{Ki}{Kp} = \frac{wp}{\tan(-\frac{pi}{2} + PMrad + tan^{-1}\left(\frac{wp}{z1}\right) + tan^{-1}\left(\frac{wp}{z2}\right) - tan^{-1}\left(\frac{wp}{p1}\right) - tan^{-1}\left(\frac{wp}{p2}\right) - tan^{-1}\left(\frac{wp}{p3}\right))} \tag{A.8}$$

$$Kp = \frac{2}{3.Vph}.\sqrt{\frac{(wp^2 + p1^2).(wp^2 + p2^2).(wp^2 + p3^2)}{(wp^2 + z1^2).(wp^2 + z2^2).(1 + \left(\frac{Ki}{wp.Kp}\right)^2)}} \tag{A.9}$$

where, $z1, z2, p1, p2$ & $p3$ are zeroes and poles of close loop transfer function of current controller.

The desired system parameters for power control loop are given below:

$$Vph = 120 * \sqrt{2} = 170V$$

Selecting open loop gain crossover frequency about two order below grid fundamental frequency,

w_c =3Hz = 18.845rad/s

PM =100deg = 628.3rad/s.

Open loop transfer function:

$$G_{OL}(s) = \frac{145.2s^4 + 1.042e05s^3 + 1.68e07\, s^2 + 7.853e08\, s}{0.0002626s^5 + 0.517s^4 + 287.7s^3 + 23800s^2} \quad \text{(A.10)}$$

Bode plot for this open loop transfer function with PI controller is shown in Figure A.2.

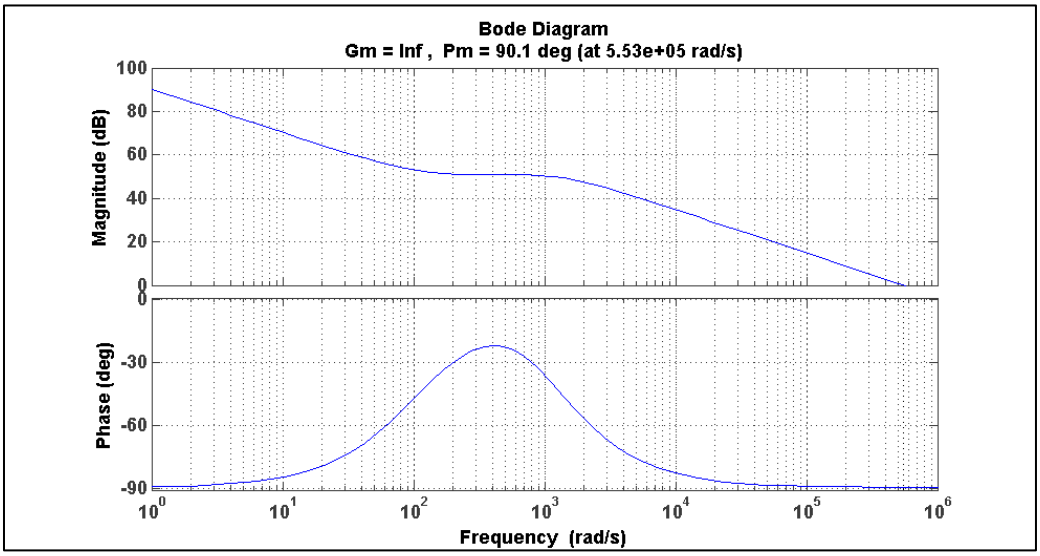

Figure A.2 Bode plot of power controller open loop TF

Close loop transfer function:

$$G_{CL}(s) = \frac{0.03812s^7 + 102.6s^6 + 1.002e5\, s^5 + 4.238e7s^4 + 7.736e9s^3 + 6.276e11s^2 + 1.87e13s}{6.896e-8s^8 + 0.03843s^7 + 103s^6 + 1.005e5s^5 + 4.2448e7s^4 + 7.749e9s^3 + 6.282e11s^2 + 1.875e13s} \quad \text{(A.11)}$$

The locations of poles and zeros of closed loop power controller are given as below,

$$P1 = 1e5 * (-5.5455)\ )$$
$$P2 = 1e5 * (-0.0094 + 0.0018i)\ )$$
$$P3 = 1e5 * (-0.0094 - 0.0018i)\ )$$
$$P4 = 1e5 * (-0.0051)\ )$$
$$P5 = 1e5 * (-0.0011)\ )$$
$$P6 = 1e5 * (-0.001)\ )$$
$$P7 = 1e5 * (-0.001)\ )$$

$$Z1 = 1e2 * (-9.359 + 1.8014i)\ )$$
$$Z2 = 1e2 * (-9.359 - 1.8014i)\ )$$
$$Z3 = 1e2 * (-5.1174)\ )$$
$$Z4 = 1e2 * (-1.0567)\ )$$
$$Z5 = 1e2 * (-1.0003)\ )$$
$$Z6 = 1e2 * (-1.0001)\ )$$

All the zeros and poles of current control closed loop are negative meaning they lie in left half plane of s-plane. Using Nyquist criteria this indicates that the closed loop system is stable.

A.3 CIRCULATING CURRENT CONTROLLER DESIGN

By using the block diagram of Figure 2-13 the equation for open loop transfer function of the current control loop between points A and B can be written as,

$$G_{OL}(s) = \left(Kp + \frac{Ki}{s}\right).\left(\frac{1}{Cpk}.\frac{1 - s.\frac{Ts}{4}}{1 + s.\frac{Ts}{4}}\right).\left(\frac{Vdc}{Ro + s.Lo}\right) \qquad \text{(A.12)}$$

The values of controller gains Kp & Ki can be found by solving equation (A.12) at desired gain crossover frequency (w_c) to achieve desired phase margin At gain crossover frequency the gain of *o*pen loop transfer function is equal to 0dB i.e. the magnitude of

equation (A.12) is equal to one. Using this criterion the equations for determining controller gains are given in equation (A.13) and (A.14).

$$\frac{Ki}{Kp} = \frac{wc}{\tan(-\frac{pi}{2} + PMrad + 2.tan^{-1}\left(\frac{wc.Ts}{4}\right) + tan^{-1}(\frac{wc.Lo}{Ro}))} \quad \text{(A.13)}$$

$$Kp = Cpk.\frac{Ro}{Vdc}.\sqrt{\frac{1+(\frac{wc.Lo}{Ro})^2}{1+(\frac{Ki}{wc.Kp})^2}} \quad \text{(A.14)}$$

Using these equations the controller gains can be determined for desired system parameters.

The desired system parameters are given below:

F_{sw}= 3000Hz and $F_{samp} = F_{sw}$

$T_{samp} = T_s = \frac{1}{F_{sw}}$

Selecting open loop gain crossover frequency same as phase current controller,

w_c =300Hz = 1884.5rad/s

Phase margin is selected to be PM=60deg in order to provide optimum trade-off between output oscillations and settling time.

Ro = 0.1 Ohm, Lo = 1mH and Vdc = 800V.

For above parameters the values of controller gains are found to be,

Kp = 1.82 and Ki = 931.85.

Open loop transfer function:

$$G_{OL}(s) = \frac{-0.002429s^2 + 27.91\,s + 1.49e04}{1.333e-06s^3 + 0.01613s^2 + 1.6\,s} \quad \text{(A.15)}$$

Bode plot for this open loop transfer function with PI controller is shown in Figure A.3.

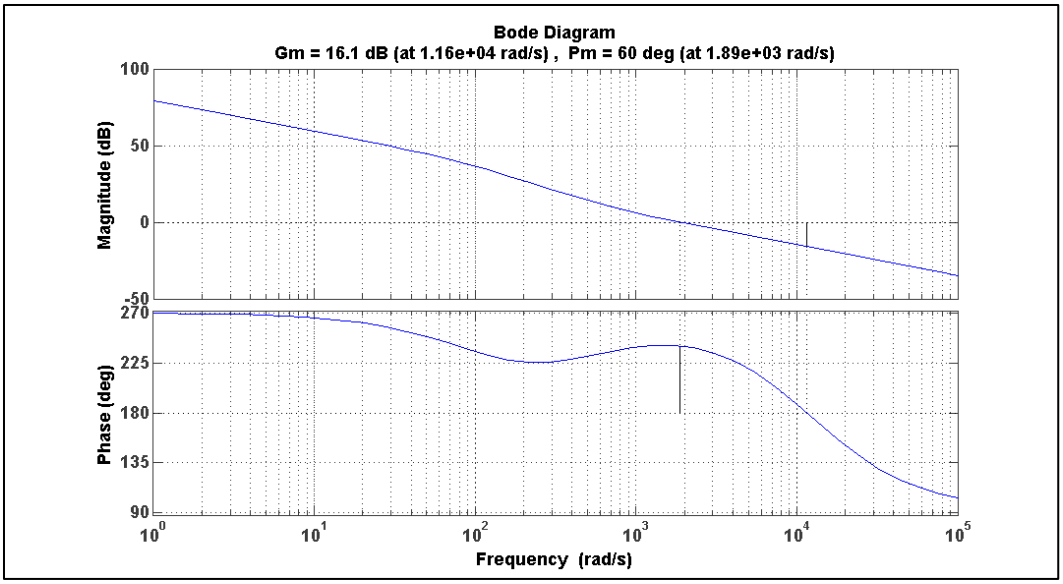

Figure A.3 Bode plot of traditional circulating current controller open loop TF

Close loop transfer function:

$$G_{CL}(s) = \frac{-3.239\text{e}-09s^5 - 1.98\text{e}-06s^4 + 0.4662s^3 + 285.2s^2 + 2.38\text{e}04\ \text{s}}{1.778\text{e}-12s^6 + 3.972\text{e}-08s^5 + 0.0002626s^4 + 0.5178s^3 + 287.7s^2 + 2.38\text{e}04\ \text{s}} \quad \text{(A.16)}$$

Neglecting some very small coefficient terms from equation (A.16),

$$G_{CL}(s) = \frac{0.466s^3 + 285.2s^2 + 2.38\text{e}04\ \text{s}}{0.0002626s^4 + 0.5178s^3 + 287.7s^2 + 2.38\text{e}04\ \text{s}} \quad \text{(A.17)}$$

The locations of poles and zeros of closed loop current controller are given as below,

$$P1 = -935$$
$$P2 = -935$$
$$P3 = -100.03$$
$$Z1 = -511.74$$
$$Z2 = -100.01$$

All the zeros and poles of current control closed loop are negative meaning they lie in left half plane of s-plane. Using Nyquist criteria this indicates that the closed loop system is stable.

APPENDIX B

DESIGN OF CPC BASED MMC CONTROLLERS

B.1 PHASE CURRENT CONTROLLER DESIGN

A first order system in Laplace domain can be represented as

$$P(s) = \left(\frac{1}{as + b}\right) \tag{B.1}$$

And a proportional-resonant controller transfer function for such system can be defined as,

$$C(s) = \left(Kp + \frac{s.Kr}{s^2 + {w_o}^2}\right) = \frac{s^2.Kp + s.Kr + Kp.{w_o}^2}{s^2 + {w_o}^2} \tag{B.2}$$

A closed loop transfer function of this system is given by,

$$G(s) = \frac{C(s)P(s)}{1 + C(s)P(s)} \tag{B.3}$$

By solving equation (B.3),

$$G(s) = \frac{s^2.Kp + s.Kr + Kp.{w_o}^2}{as^3 + (b + Kp)s^2 + (a{w_o}^2 + Kr)s + {w_o}^2(b + Kp)} \tag{B.4}$$

For this closed loop transfer function a 3rd order Naslin equivalent polynomial is given by,

$$N(s) = a_0\left(1 + s\tau + s^2\frac{\tau^2}{\alpha} + s^3\frac{\tau^3}{\alpha^3}\right) \tag{B.5}$$

By matching the coefficients of equation (B.4) denominator (characteristic polynomial) and equation (B.5) the solution for system time constant and controller gains is found and it is given by equation (B.6).

$$\tau = \frac{\sqrt{\alpha}}{w_0}; \quad Kp = a\frac{\alpha^3}{\tau} - b; \quad Kr = a\left(\frac{\alpha^3}{\tau^2} - {w_0}^2\right) \tag{B.6}$$

Where, τ is system time constant, w_0 is resonant frequency.

$\alpha = 4 * \xi^2$; ξ is damping factor and α is characteristic ratio.

Using this method the PR controller can be designed for phase current controllers.

The open loop transfer function of MMC is given by,

$$P(s) = PWM(s) * \left(\frac{Gt}{Cpk}\right) * MMC(\mathrm{s}) \tag{B.7}$$

$$P(s) = \left(\frac{1}{Cpk}.\frac{1 - s.\frac{Ts}{4}}{1 + s.\frac{Ts}{4}}\right).\left(\frac{2Vdc}{Ro + s.Lo}\right) \tag{B.8}$$

For this system the proportional resonant controller transfer function remains the same as in equation (B.2). The closed loop transfer function with PR controller and MMC can then be written as,

$$G(s) = \frac{C(s)P(s)}{1 + C(s)P(s)} \tag{B.9}$$

$$G(s) = \frac{s^2.Kp + s.Kr + Kp.{w_o}^2}{\left(\frac{Lo}{G}\right)s^3 + \left(\frac{Ro}{G} + Kp\right)s^2 + \left(\frac{{w_o}^2 Lo}{G} + Kr\right)s + {w_0}^2\left(\frac{Ro}{G} + Kp\right)} \quad \text{(B.10)}$$

where,

$$G = \frac{2Vdc}{Cpk} \quad \text{(B.11)}$$

The characteristic polynomial of equation (B.10) is given by,

$$D(s) = \left(\frac{Lo}{G}\right)s^3 + \left(\frac{Ro}{G} + Kp\right)s^2 + \left(\frac{{w_o}^2 Lo}{G} + Kr\right)s + {w_0}^2\left(\frac{Ro}{G} + Kp\right) \quad \text{(B.12)}$$

Representing equation (B.12) in the same form as equation (B.5) i.e. Naslin Polynomial,

$$D(s) = {w_0}^2\left(\frac{Ro}{G} + Kp\right)\left[1 + s\frac{\left(\frac{{w_o}^2 Lo}{G} + Kr\right)}{{w_0}^2\left(\frac{Ro}{G} + Kp\right)} + s^2\frac{\left(\frac{Ro}{G} + Kp\right)}{{w_0}^2\left(\frac{Ro}{G} + Kp\right)} + s^3\frac{\left(\frac{Lo}{G}\right)}{{w_0}^2\left(\frac{Ro}{G} + Kp\right)}\right] \quad \text{(B.13)}$$

Comparing coefficients of equation (B5.) and equation (B.13) the system time constant and controller gains is found as given by equations (B.14) - (B.16)

$$\tau = \frac{\sqrt{\alpha}}{w_0} \quad \text{(B.14)}$$

$$Kp = \frac{1}{G}\left(\frac{L_o \alpha^2}{\tau} - R_o\right) \quad \text{(B.15)}$$

$$Kr = \frac{1}{G}({w_0}^2[\tau(R_0 + KpG)] - L_o) \quad \text{(B.16)}$$

Selecting $\xi = 0.8$ gives $\alpha = 2.56$ & $\tau = 0.0042sec$; $w_0 = 2 * pi * 60$ and using given system parameters similar to control design in chapter 2 the controller gains are found to be, $Kp = 0.7221$ & $Kr = 394.64$.

Putting the values of gains in the Proportional-resonant controller transfer function it becomes,

$$C(s) = \left(0.7721 + \frac{s.394.64}{s^2 + 377^2}\right) \tag{B.17}$$

Using equation (B.8), (B.17) and given system parameters the open loop transfer function of CPC phase current control loop with controller is obtained as,

$$G_{OL}(s) = \frac{-0.001926s^3 + 22.05s^2 + 1.235e4s + 3.284e6}{1.33e-6s^4 + 0.01613s^3 + 1.789s^2 + 2293s + 2.27e5} \tag{B.18}$$

Bode plot for this open loop transfer function with PR controller is shown in Figure B.1.

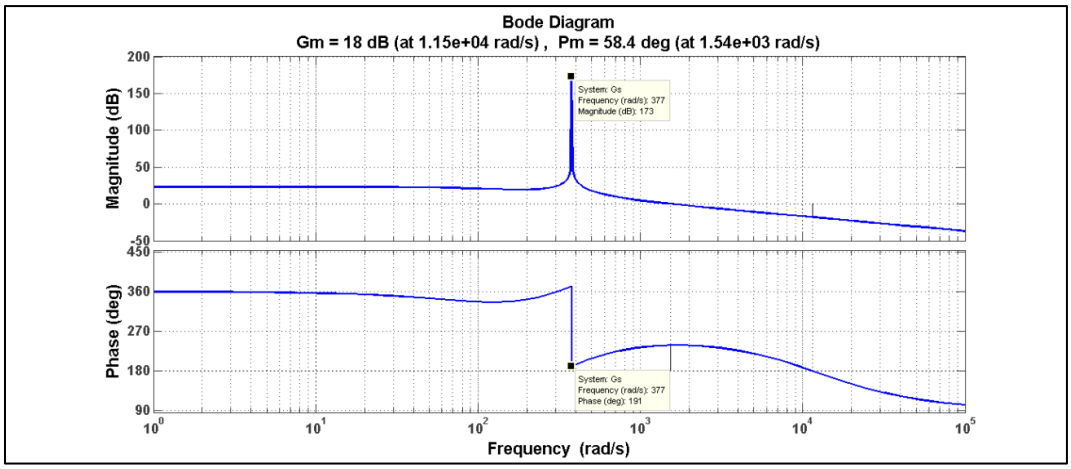

Figure B.1 Bode plot of CPC phase current control loop

The closed transfer function then obtained as,

$$G_{CL}(s) = \frac{-2.567e-9s^7 - 1.66e-6s^6 + 0.3688s^5 + 238.8s^4 + 1.252e5s^3 + 3.92e7s^2 + 1.034e10s + 7.468e11}{1.77e-12s^8 + 4.045e-8s^7 + 0.0002634\,s^6 + 0.4327s^5 + 316.5s^4 + 1.408e5s^3 + 4.529e7s^2 + 1.138e10s + 7.985e11} \tag{B.19}$$

The poles and zeros of closed loop transfer function (B.19) are found to be,

$$P1 = -(1e4) * (1.2)$$
$$P2 = -(1e4) * (0.875)$$
$$P3 = -(1e4) * (0.0956)$$
$$P4 = -(1e4) * (0.0474 + 0.03j)$$
$$P5 = +(1e4) * (0.0474 - 0.03j)$$
$$P6 = -(1e4) * (0.0377j)$$
$$P7 = -(1e4) * (-0.0377j)$$
$$P8 = -(1e4) * (0.01)$$

$$Z1 = +(1e4) * (1.2)$$
$$Z2 = -(1e4) * (1.2)$$
$$Z3 = +(1e4) * (0.0377j)$$
$$Z4 = -(1e4) * (0.0377j)$$
$$Z5 = -(1e4) * (0.0273 + 0.026j)$$
$$Z6 = -(1e4) * (0.0273 - 0.026j)$$
$$Z7 = -(1e4) * (0.01)$$

From above, P1 & Z2, P6 & Z3, P7 & Z4, P8 & Z7 cancel out each other. Zero Z1 is on the right half of plane. There is a pair of complex poles (P5, P6) on the imaginary axis which makes system marginally stable. But no poles are in the right half plane of the s-plane. Therefore, using the bode plot of Figure B-1 it is found that both gain margin and phase margin are positive and acceptable and knowing that there are no poles in right half plane of s-plane therefore the closed loop system is stable.

Using Laplace to z-transformation, equation (B.17) can be converted into discrete domain for digital implementation. The discrete transfer function of controller is given by equation (B.20) and (B.21).

$$C(z) = \left(Kp + Kr * T * \frac{z(z - \cos(w_0 T)}{z^2 - 2\cos(w_0 T) + 1} \right) \tag{B.20}$$

$$C(z) = \left(0.7721 + 0.1315 \frac{z^2 - 0.9921z)}{z^2 - 1.984z + 1} \right) \tag{B.21}$$

B.2 CIRCULATING CURRENT CONTROL DESIGN

$$G(s) = \frac{s^2.Kp + s.Kr + Kp.{w_o}^2}{\left(\frac{Lo}{G}\right)s^3 + \left(\frac{Ro}{G} + Kp\right)s^2 + \left(\frac{{w_o}^2 Lo}{G} + Kr\right)s + {w_0}^2\left(\frac{Ro}{G} + Kp\right)} \quad \text{(B.22)}$$

This is same as equation (B.10) except that the value of G is different. For circulating current control loop G is given by,

$$G = \frac{Vdc}{Cpk} \quad \text{(B.23)}$$

Since closed loop transfer function format is same as phase current control loop the characteristic polynomials can be derived from equations (B.11) & (B.12). The system time constant and controller gains are then found using equation (B.14), (B.15) & (B.16).

Selecting $\xi = 0.65$ gives $\alpha = 1.69$ & $\tau = 0.0017sec$; $w_0 = 2 * pi * 120$ and using given system parameters similar to control design in chapter 2 the controller gains are found to be,

$Kp = 1.5565$ & $Kr = 1.0552e3$.

Putting the values of gains in the Proportional-resonant controller transfer function it becomes,

$$C(s) = \left(1.5565 + \frac{s.1055}{s^2 + 754^2}\right) \quad \text{(B.24)}$$

Using equation (B.8), (B.22) and given system parameters same as in chapter 2 control design the closed loop transfer function of CPC phase current control loop is obtained as,

$$G_{OL}(s) = \frac{-0.002075s^3 + 23.5s^2 + 1.57e4s + 1.416e7}{1.33e-6s^4 + 0.01613s^3 + 2.358s^2 + 9172s + 9.096e5} \quad \text{(B.25)}$$

Bode plot for this open loop transfer function with PR controller is shown in Figure B.2.

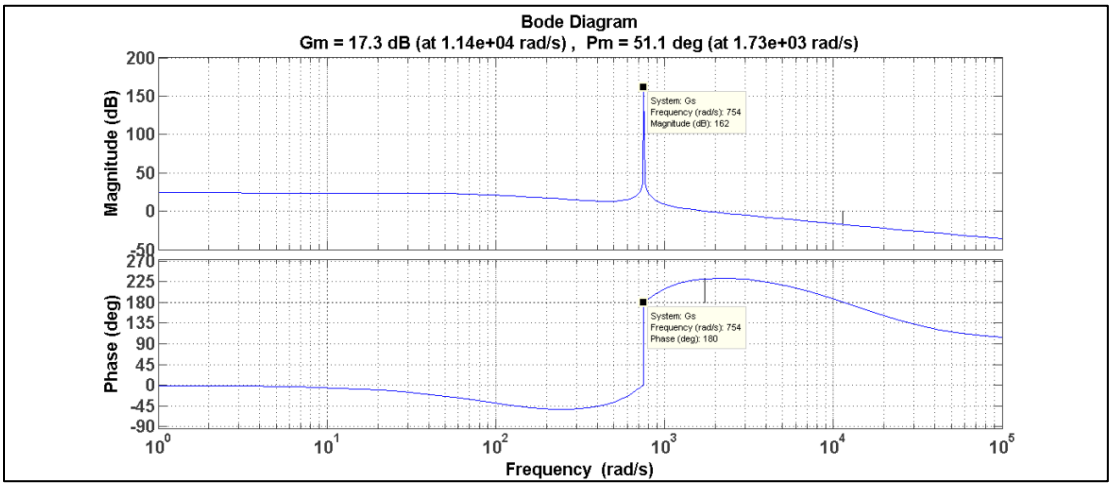

Figure B.2 Bode plot of PR circulating current controller loop

The closed transfer function then obtained as,

$$G_{CL}(s) = \frac{-2.767e-9s^7 - 2.153e-6s^6 + 0.3951s^5 + 308.6s^4 + 4.791e5s^3 + 1.988e8s^2 + 1.441e11s + 1.288e13}{1.778e-12s^8 + 4.026e-8s^7 + 0.0002644\,s^6 + 0.4957s^5 + 612.5s^4 + 5.517e5s^3 + 2.872e8s^2 + 1.608e11s + 1.37e13} \quad \text{(B.26)}$$

The poles and zeros of closed loop transfer function (B.24) are found to be,

$$P1 = -(1e4) * (1.2)$$
$$P2 = -(1e4) * (0.8503)$$
$$P3 = -(1e4) * (0.1261)$$
$$P4 = -(1e4) * (0.039 + 0.095j)$$
$$P5 = +(1e4) * (0.039 - 0.095j)$$
$$P6 = -(1e4) * (0.0754j)$$
$$P7 = -(1e4) * (-0.0754j)$$
$$P8 = -(1e4) * (0.01)$$

$$Z1 = +(1e4) * (1.2)$$
$$Z2 = -(1e4) * (1.2)$$
$$Z3 = +(1e4) * (0.0754j)$$
$$Z4 = -(1e4) * (0.0754j)$$
$$Z5 = -(1e4) * (0.0339 + 0.0673j)$$
$$Z6 = -(1e4) * (0.0339 - 0.0673j)$$
$$Z7 = -(1e4) * (0.01)$$

From above, P1 & Z2, P6 & Z3, P7 & Z4, P8 & Z7 cancel out each other. Zero Z1 is on the right half of plane. There is a pair of complex poles (P5, P6) on the imaginary axis which makes system marginally stable. But no poles are in the right half plane of the s-plane. Therefore, using the bode plot of Figure B-2 it is found that both the gain margin and phase margin are positive and acceptable and knowing that there are no poles in right half plane of s-plane therefore the closed loop system is stable.

Using Laplace to z-transformation, controller transfer function can be converted into discrete domain for digital implementation. Using similar formula as in equation (B.20) the discrete transfer function of controller is given by,

$$C(z) = \left(1.5565 + 0.351\frac{z^2 - 0.968z)}{z^2 - 1.937z + 1}\right) \tag{B.27}$$

APPENDIX C

ESTIMATION OF IGBT AND DIODE PARAMETERS

This section explains computation of various IGBT and Diode parameters using datasheet. Semikron SEMiX252GB126HDs IGBT is selected. This IGBT can handle 1.2kV forward voltage and 170A collector current at 80deg C.

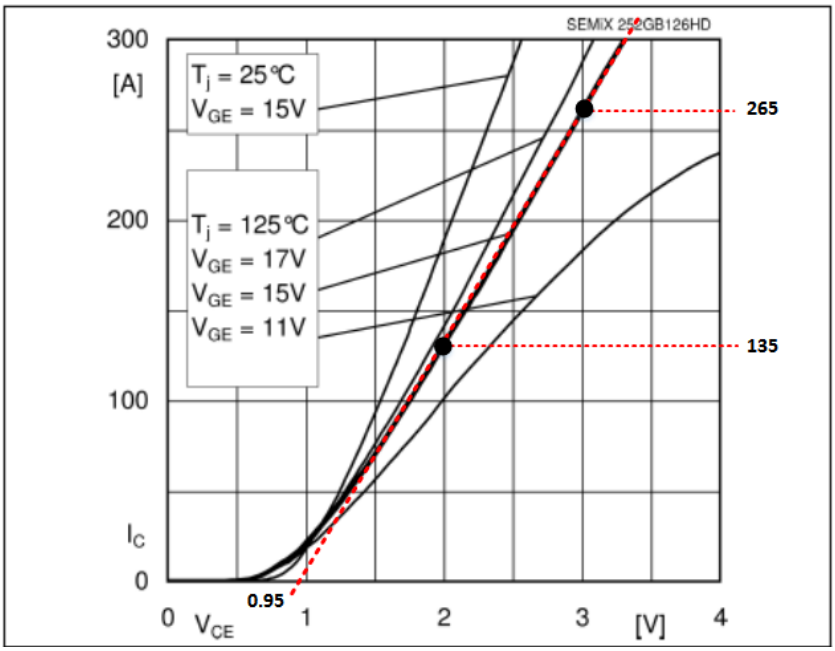

Figure C.1 IGBT Forward Characteristics

IGBT ON resistance:

$$R_{CE} = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{3-2}{265-135} = 7.7mOhm$$

IGBT Collector-Emitter voltage for zero Collector current:

$$V_{CE0} = 0.95V$$

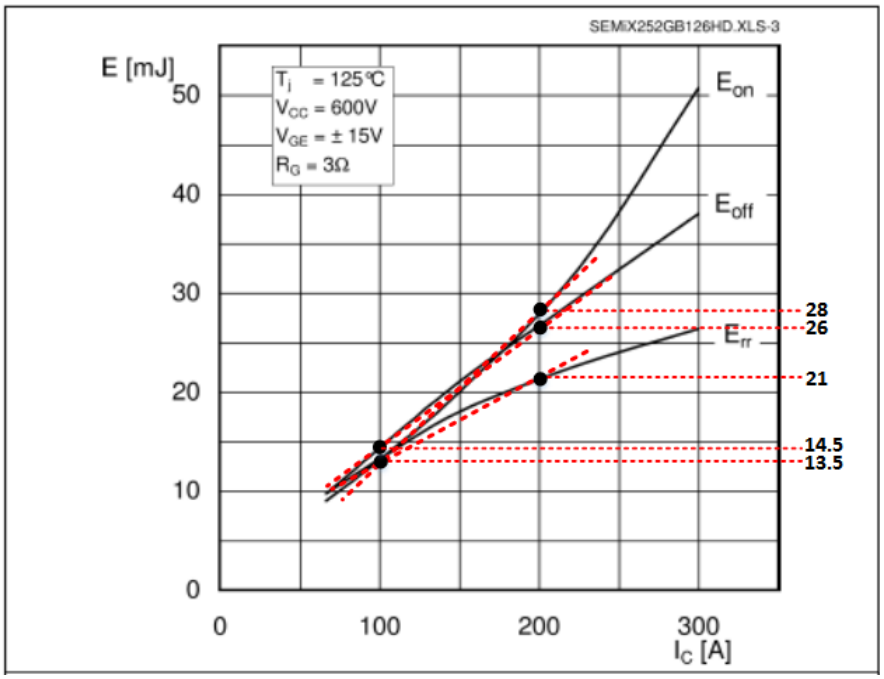

Figure C.2 Turn ON/OFF Energy Loss

Estimated IGBT Turn-on Energy loss slope:

$$K_{ON} = \frac{\Delta E_{ON}}{\Delta I_c} = \frac{(28 - 13.5) * 10^{-3}}{200 - 100} = 145 * 10^{-6}$$

Estimated IGBT Turn-off Energy loss slope

$$K_{OFF} = \frac{\Delta E_{OFF}}{\Delta I_c} = \frac{(26 - 14.5) * 10^{-3}}{200 - 100} = 115 * 10^{-6}$$

Estimated Diode reverse recovery Energy loss slope

$$K_{rr} = \frac{\Delta E_{rr}}{\Delta I_c} = \frac{(21 - 13.5) * 10^{-3}}{200 - 100} = 75 * 10^{-6}$$

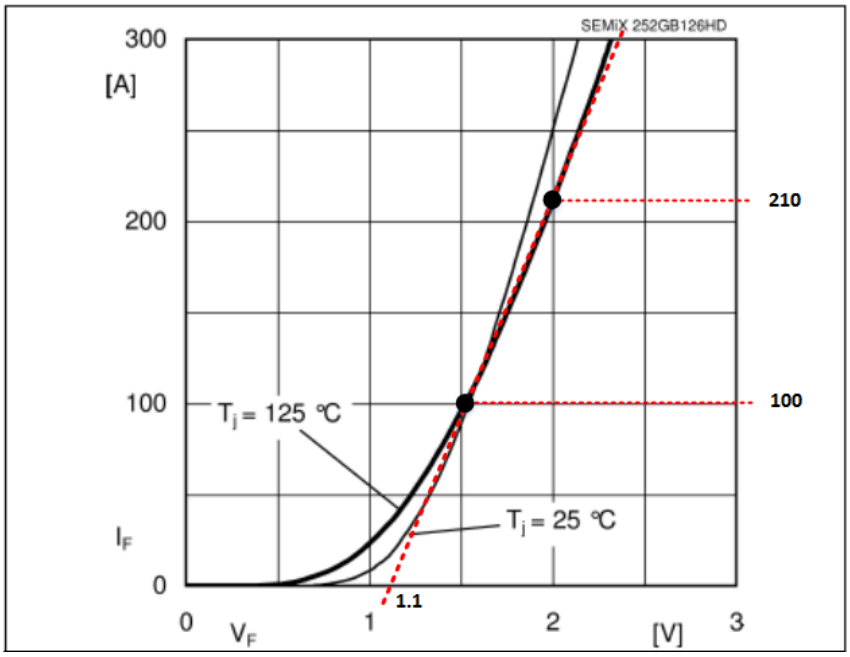

Figure C.3 Diode Forward Characteristics

Diode forward resistance:

$$R_D = \frac{\Delta V_D}{\Delta I_D} = \frac{2 - 1.5}{210 - 100} = 4.5mOhm$$

Diode forward voltage for zero Collector current:

$$V_{D0} = 1.1V$$